SCHEME OF INSTRUCTION & EXAMINATION
B.E. II YEAR
COMPUTER SCIENCE & ENGINEERING

SEMESTER - I

Sl. No.	Syllabus Ref. No.	SUBJECT	Scheme of Instruction		Scheme of Examination		
			Periods per week		Duration In Hours	Maximum Marks	
			L	D/P		Univ. Exam	Sessionals
		THEORY					
1.	MT 201	Mathematics-III	4	-	3	75	25
2.	CS 201	Data Structures using C++	4	-	3	75	25
3.	CS 202	Discrete Structures	4	-	3	75	25
4.	CS 203	Logic and Switching Theory	4	-	3	75	25
5.	CS 204	Computer Architecture	4	-	3	75	25
6.	EC 222	Basic Electronics	4	-	3	75	25
		PRACTICALS					
1.	CS 231	Data Structures Lab using C++	-	3	3	50	25
2.	EC 242	Basic Electronics Lab	-	3	3	50	25
		TOTAL	**24**	**6**	**24**	**550**	**200**

MT 201

MATHEMATICS-III
(Common to all Branches)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Partial differential Equations : Formation of partial-differential equation of first order-Lagrange's solution, Standard types-Charpit's method of solution-partial differential equations of higher order, Monge's method.

UNIT-II

Fourier Series : Expansion of a function in Fourier series for a given range-odd and even functions of Fourier series-change of interval-Applications of Fourier series-square wave forms-saw tooth wave form and modified square saw tooth wave form-half range sine and cosine expansions-complex Fourier series.

UNIT-III

Applications of Partial differential equations : Solution of wave equation, hear equation and Laplace's equation by the method of separation of variables and their use in problems of vibrating string, one dimensional unsteady heat flow and two dimensional steady state hear flow.

UNIT-IV

Numerical methods : Solutions of Algebraic and Transcendental equations - Bisection method, Regula-Falsi method and Newton-Raphson's method-Solution of Linear system of equations, Gauss elimination method, Gauss Seidel iterative method, ill conditioned equations and refinement of solutions, Interpolation, Newton's divided difference interpolation-Numerical differentiation, Solution of differential equations by Euler's method, modified Euler's method and Runge-Kutta Method of 4th order.

UNIT-V

Z-Transforms : Introduction, Basic Theory of Z-transforms. Z-transform of some standard sequences, Existence of Z-Transform. Linearity property, Translation Theorem, Scaling property, Initial and Final Value Theorems, Differentiation of Z-Transform, Convolution Theorem, Solution of Difference equations using Z-transforms.

Suggested Reading:

1. R.K. Jain & S.R.K. Iyengar, *Advance Engineering Mathematics,* Narosa Publications - 2008.
2. B.S. Grewal, *Higher Engineering Mathematics,* Khanna Publications, 40th Edition, 2008.
3. N. Bali, M.Goyal, C.Watkins, *Advanced Engineering Mathematics,* 7th Edition, 2009 Laxmi Publications.
4. M.K. Venkatraman, *Engineering Mathematics-III,* Technical Publications, Chennai.
5. H.K. Dass, *Advanced Engineering Mathematics,* S.Chand & Co. Pvt. Ltd., 2010.

CS 201

DATA STRUCTURES USING C++

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Algorithm Specification, Performance Analysis and Measurement.

Arrays: Abstract Data Types and the C++ Class, The Array as an Abstract Data Type, The Polynomial Abstract Data Type, Sparse Matrices, Representation of Arrays, The String Abstract Data Type.

UNIT-II

Stacks and Queues: Templates in C++, The Stack Abstract Data Type, The Queue Abstract Data type, Subtyping and Inheritance in C++, A Mazing Problem, Evaluation of Expressions, Additional Exercises.

UNIT-III

Linked Lists: Singly Linked Lists and Chains, Representing Chains in C++, The Template Class Chain, Circular Lists, Available Space Lists, Linked Stacks and Queues, Polynomials, Equivalence Classes, Sparse Matrices, Doubly Linked Lists, Generalized Lists.

UNIT-IV

Trees: Introduction, Binary Trees, Binary Tree Traversal and Tree Integrators, Copying Binary Trees, Threaded Binary Trees, Heaps, Binary Search Trees.

Graphs: The Graph Abstract Data Type, Elementary Graph operations (dfs and bfs), Minimum Cost Spanning Trees (Prim's and Kruskal's Algorithms).

UNIT-V

Sorting: Insertion sort, Quick sort, How Fast Can We Sort, Merge sort, Heap sort, Sorting on Several Keys, List and Table Sorts, Summary of Internal Sorting.

Hashing: Static Hashing.

Efficient Binary Search Trees: AVL Trees, Red-Black Trees, Splay Trees, m-way Search Trees, B-Trees.

Suggested Reading:

1. Ellis Horowitz, Dinesh Mehta, S. Sahani. *Fundamentals of Data Stuctures in C++,* Universities Press. 2007.
2. T.H. Cormen, C.E. Leiserson, and R.L. Rivest. *Introduction to Algorithms,* Prentice Hall of India 1996.
3. Mark Allen Weiss, *Data Structures and Algorithm Analysis in C++,* Pearson Education 2006.

CS 202

DISCRETE STRUCTURES

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Fundamentals of Logic: Basic Connectives and Truth Tables, Logical Equivalence, Logical Implication, Use of Quantifiers, Definitions and the Proof of Theorems.

Set Theory: Set and Subsets, Set Operations, and the Laws of Set theory, Counting and Venn Diagrams.

Properties of the Integers: The well – ordering principle, Recursive definitions, the division algorithms, fundamental theorem of arithmetic.

UNIT-II

Relations and Functions: Cartesian Product, Functions onto Functions, Special Functions, Pigeonhole Principle, Composition and Inverse Functions, Computational Complexity.

Relations: Partial Orders, Equivalence Relations and Partitions.

Principle of Inclusion and Exclusion: Principles of Inclusion and Exclusion, Generalization of Principle, Derangements, Rock Polynomials, Arrangements with Forbidden Positions.

UNIT-III

Generating Functions: Introductory examples, definition and example Partitions of Integers, exponential generating function, summation operator.

Recurrence Relations: First – order linear recurrence relation, second – order linear homogenous recurrence relation with constant coefficients, Non homogenous recurrence relation, divide and conquer algorithms.

UNIT-IV

Algebraic Structures: Algebraic System – General Properties, semi groups, Monoids, homomorphism, Groups, Residue arithmetic, group codes and their applications.

UNIT-V

Graph Theory: Definitions and examples, subgraphs, complements and graph Isomorpshim, Vertex degree, Planar graphs, Hamiltonian paths and Cycles, Graph Coloring.

Trees: Definitions, properties and Examples, Rooted Trees, Spanning Trees and Minimum Spanning Trees.

Suggested Reading:

1. Ralph P.Grimaldi, *Discrete and Combinatorial Mathematics,* 4th edition, 2003, Pearson Education.
2. J.P.Tremblay, R.Manohar, *Discrete Mathematical Structure with Applications to Computer Science*, McGraw Hill, 1987.
3. Joe L.Mott, A.Kandel, T.P.Baker, *Discrete Mathematics for Computer Scientists & Mathematicians,* Prentice Hall N.J., 1986.
4. Thomas Koshy, *Discrete Mathematics with Applications,* Elsevier Inc.2004.

CS 203

LOGIC AND SWITCHING THEORY

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Digital Computers and Information: Information representation, Computer Structure.

Number Systems: Binary Numbers, Octal and Hexadecimal Numbers, Number Ranges.

Arithmetic Operations: Conversion from Decimal to other bases.

Decimal Codes: BCD Addition. Alphanumeric Codes: ASCII Character Code, Parity Bit.

Binary Logic and Gates: Binary Logic, Logic Gates. Boolean Algebra: Basic Identifiers, Algebraic Manipulation, Complement of a Function.

Standard Forms: Minterms and Maxterms, Sum of Product and Products of Sums.

UNIT-II

Minimization of Switching Functions: Introduction, the map method, Minimal Functions and Their Properties, the tabulation procedure, the prime implicant chart.

NAND and NOR Gates: Nand Circuits, Two-level Implementation, Multilevel NAND Circuits, NOR Circuits. Exclusive OR Gates: Odd Function, Parity Generation and Checking.

UNIT-III

Combination Logic Design: Combinational Circuits, Design Topics: Design Hierarchy, Top –Down design, Computer Aided Design, Hardware Description Languages, Logic Synthesis. Analysis Procedure: Derivation of Boolean Functions, Derivation of the Truth Table, Logic Simulation, Design Procedure, Decoders, Encoders, Multiplexers, Binary Adders, Binary subtraction, Binary Multipliers, HDL Representations- VHDL.

UNIT-IV

Sequential Circuits: Sequential Circuit definitions. Latches, Flip Flops, sequential circuit analysis, sequential circuit design, design with D Flip Flops, designing with JK Flip- Flops, HDL representation for sequential circuits-VHDL.

UNIT-V

Registers and Counters: Registers, Shift registers, Synchronous Binary counters, Ripple Counter.

Symmetric Networks: Properties of Symmetric Functions, Synthesis of Symmetric networks, identification of symmetric functions.

Suggested Reading:

1. M. Moris Mano, Charles R. Kime, *Logic and Computer Design Fundamentals,* 2nd edition, Pearson Education Asia, 2001.
2. Zvi Kohavi, *Switching and Finite Automata Theory,* 2nd edition, Tata McGraw Hill, 1995.
3. Charles H. Roth, J*r Fundamentals of Logic Design,* 5th edition, Thomson, Brook,Cole, 2005.

CS 204

COMPUTER ARCHITECTURE

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Register Transfer and Microoperations: Register transfer language, Register Transfer, Bus and, Memory Transfers, Arithmetic Microoperations: Binary Adder, Subtractor, Binary Incrementer, Arithmetic Circuit. Logic Microoperations: List of Logic Microoperations, hardware Implementation. Arithmetic. Logic Shift unit.

Basic Computer Organization and Design: Instruction Codes: Stored program organization, Indirect Address. Computer Registers: Common Bus System. Computer Instructions: Instruction Set Completeness. Timing and Control, Instruction Cycle: Fetch and Decode, Register Reference Instructions. Memory Reference Instructions: Example Instructions, Control Flow Chart. Input-Output and Interrupt: Configuration, Instructions, Program Interrupt, Interrupt Cycle. Complete Computer Description. Design of Basic Computer, Basics of Accumulator Logic.

UNIT-II

Microprogrammed Control: Control Memory, Address Sequencing: Control Branching Mapping of Instruction, Subroutines. Microprogram Example: Computer Configuration, Microinstruction Format, Symbolic Microinstructions.The Fetch Routine, Symbolic Microprogram, Binary Microprogram. Design of Control Unit: Microprogram Sequencer Central Processing Unit: General Register Organization: Control World Stack Organization: Register Stack, Memory Stack, Reverse Polish Notation, Evaluation of Expressions. Instruction Formats: Three, Two, One, Zero Address Instructions, RISC Instructions. Addressing Modes. DataTransfer and Manipulation: Data Transfer Instructions, Data Manipulation Instruction, Arithmetic Instruction Logical, Shift and Bit Manipulation Instructions.

Program Control: Status Bit Conditions, Conditional Branch Instructions Subroutine Call and Return, Program Interrupt, Types of Interrupts, Reduced Instruction Set Computer: CISC.

Characteristics, RISC Characteristics, Overlapped Register Windows.

UNI-III

Pipeline and Vector Processing: Parallel Processing, Pipelining, Instruction Pipeline, RISC Pipeline, Vector Processing: Vector Operations, Matrix Multiplication, Memory Interleaving, Super Computers. Array Processors: Attached Array Processor, SIMD Array Processor.

Computer Arithmetic: Addition and Subtraction: With Signed Magnitude Data, Implementation and algorithm, Addition and Subtraction with 2's Complement Data. Multiplication Algorithms with signed magnitude data, algorithm, Booth's algorithm, Array multiplier. Division Algorithms with signed magnitude data, divide overflow, algorithm. Floating Point Arithmetic Operations, Decimal Arithmetic Unit: BCD Adder, Subtractor.

UNIT-IV

Input Output Organization: Input-Output Interface: I/O Bus and Interface Modqles, I/O Versus Memory Bus, Isolated vs Memory Mapped I/O. Asynchronous Data Transfer: Strobe Control, Handshaking, Asynchronous Serial Transfer, Asynchronous Communication Interface.

Modes of Transfer: Programmed I/O, Interrupt driven I/O. Priority Interrupt: Daisy Chaining, Parallel Priority Interrupt, priority Encoder. Direct Memory Access: DMA Controller and Transfer. Input-Output Processor (lOP): CPU-IOP Communication, IBM 370 I/O Channel, Intel 8089-IOP. Serial Communication.

UNIT-V

Memory Organization: Memory Hierarchy, Main Memory: RAM and ROM Chips, Address Map, Memory Connection to CPU. Auxiliary Memory: Disks and Tapes. Associative Memory: Hardware Organization, Match Logic, Read. Operation and Write Operation. Cache

Memory: Associative Mapping, Direct. Mapping, Set-Associative Mapping, Writing into Cache Initialization. Virtual Memory: Address and Memory Space, Address Mapping, Page Replacement.

Suggested Reading:

1. M. Morris Mano, *Computer System Architecture,* 3rd edition, Pearson Education Asia, 2002.
2. William Stallings, *Computer Organization & Architecture*, 6th Edition, Pearson Education Asia, 2003.
3. V.Carl Hamacher, Z.G Vranesic, S.G. Zaky, *Computer Organization,* McGraw Hill, 2004.
4. David A. Patterson, John L. Hennessy, *Computer Organization and Design.* Morgan, Elsevier Inc, 2009.

EC 222

BASIC ELECTRONICS
(For Mech., Prod., and CSE)
(Same as EC 222)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Semi Conductor Theory: Energy Levels, Intrinsic and Extrinsic Semiconducts, Mobility, Diffusion and Drift current. Hall Effect, Characteristics of P-N Junction diode, Parameters and Applications.

Rectifiers: Half wave and Full wave Rectifiers (Bridge, center tapped) with and without filters, ripple regulation and efficiency.

UNIT-II

Transistors: Bipolar and Field effect transistors with their h-parameters equivalent circuits. Basic amplifiers classification and their circuits (Qualitative treatment only).

Regulators and Inverters: Zener Diode regulator, Transistorized an IC regulators and Simple Inverter Circuits.

UNIT-III

Feedback Concepts – Properties of Negative Feedback Amplifiers, Classification, Parameters Applications.

Oscillators – LC Type and RC Type Oscillators and Crystal Oscillators (Qualitative treatment only)

UNIT-IV

Operational Amplifiers - Basic Principle – Characteristics and Applications (Summer Adder, Integrator, Differentiator, Instrumentation Amplifier).

Digital Systems: Basic Logic Gates, half, Full Adder and Subtractors.

UNIT-V

Data Acquisition systems: Study of transducer (LVDT, Straingauge, Temperature, Force). **Photo Electric Devices and Industrial Devices:** Photo diode, Photo Transistor, LED, LCD, SCR, TRAIC, DIAC, UJT Construction and Characteristics only.

Display Systems: Constructional details of C.R.O and Applications.

Suggested Reading:

1. Jocob Millman, Christos C. Halkias and Satyabrata Jit, Electronics Devices and Circuits, McGraw Hill, 3/e., 2010.
2. Rama Kanth A. Gaykward, *Op-AMPS and Linear Integrated Circuits* -, EEE, 3/e., 1998.(Ch 2, 3 & 7).
3. Moris Mano, *Digital Design, PHI, 3/e., 2009.* (2,4 Chapters)
4. Cooper, *Electronic Measurements and Instrumentations, 3/e., 1998.* (Ch 7)
5. S.Shalivahnan, N. Suresh Kumar, A Vallavea Raj, *Electronic Devices and Circuits,* TMH, 2003.

CS 231

DATA STRUCTURES LAB USING C++

Instruction	3	Periods per week
Duration of University Examination	3	Hours
University Examination	50	Marks
Sessional	25	Marks

List of Experiments:

1. Implementation of Stacks, Queues.
2. Infix to Postfix Conversion, evaluation of postfix expression.
3. Polynomial arithmetic using linked list.
4. Implementation of Binary Search and Hashing.
5. Implementation of Selection, Shell, Merge and Quick sorts.
6. Implementation of Tree Traversals on Binary Trees.
7. Implementation of Heap Sort.
8. Implementation of operations on AVL Trees.
9. Implementation of Traversal on Graphs.
10. Implementation of Splay Trees.

Note: For each of the problems PSP (Personal Software Process) Principles should be applied.

EC 242

BASIC ELECTRONICS LAB
(For Mech., Prod. & CSE)

Instruction	3	Periods per week
Duration of University Examination	3	Hours
University Examination	50	Marks
Sessional	25	Marks

1. Characteristics of Semiconductor and Zener diodes
2. CRO Applications
3. Fullwave rectifier with and without filter
4. Zener Voltage Regulator
5. Characteristics of BJT transistor (CB.CE.CC)
6. Characteristics of field effect transistor.
7. Feedback amplifier and amplifier without feedback
8. h-parameters of transistors
9. Phase shift oscillator
10. Hartley oscillator & Calpitts Oscillator.
11. Operational Amplifier and it's applications
12. Logic gates and flip flops-verifications
13. Realization of Half and Full adder
14. Comparators

Suggested Reading :

1. Paul B. Zbar, Albert P. Malvino , Michael A. Miller, *Basic Electronics, A Text-Lab Manual,* 7th Edition, TMH, 1994.
2. Paul B. Zbar, *Industrial Electronics, A Text – Lab Manual,* 3rd Edition, TMH, 1983.

General Note :

1. There should not be more than 2 students per batch while performing any of the lab experiment.
2. Mini Project cum design exercise :
   a) The students must design, rig-up, and test the circuits wherever possible and should carry out the experiments individually.
   b) This exercise carries sessional marks of 10 out of 25, while the remaining 15 marks are for the remaining lab exercises.