SCHEME OF INSTRUCTION & EXAMINATION

B.E. IIIrd YEAR
(ELECTRICAL AND ELECTRONICS ENGINEERING)

SEMESTER-I

Sl. No.	Syllabus Ref. No.	SUBJECT	Scheme of Instruction		Scheme of Examination		
			Periods per week		Duration In Hours	Maximum Marks	
			L/T	D/P		Univ. Exam	Sessionals
		THEORY					
1.	EE 301	Power Systems - II	4	-	3	75	25
2.	EE 302	Electrical Machinery - II	4/1	-	3	75	25
3.	EE 303	Power Electronics	4/1	-	3	75	25
4.	EE 304	Digital Electronics and Logic Design	4	-	3	75	25
5.	EE 305	Linear Integrated Circuits	4	-	3	75	25
6.	EE 306	Linear Control Systems	4 /1	-	3	75	25
		PRACTICALS					
1.	EE 331	Electrical Machines Lab-I	-	3	3	50	25
2.	EE 332	Control Systems Lab	-	3	3	50	25
		Total	**24/3**	**6**	**24**	**550**	**200**

EE 301

POWER SYSTEMS - II

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Transmission Line theory: Short, medium, long lines- Line calculations, Tuned Lines-Power Circle Diagrams and their applications. Corona: Causes- Disruptive and Visual Critical Voltages, Power loss -minimization of Corona effects.

UNIT-II

Voltage Control: Phase Modifiers, Induction Regulators -Tap Changing Transformers, Series and Shunt Capacitance. Reactive Power Requirement Calculations. Static Var Compensators-Thyristor Controlled Reactors-Thyristor Switched Capacitors.

UNIT-III

Per Unit System of Representation: Use of per unit quantities in power systems, Advantages of per unit system. Symmetrical Three Phase transients in R-L series circuits- Short Circuit Currents - Reactance of Synchronous Machines- Symmetrical Fault Calculations. Short circuit capacity of a bus.

UNIT-IV

Unsymmetrical Faults: Symmetrical components of unsymmetrical phasors -Power in terms of symmetrical components -sequence impedance and sequence networks. Sequence networks of unloaded generators - Sequence impedances of circuit elements -Single line to ground, line-to-line and double line to ground faults on unloaded generator- Unsymmetrical faults of power systems.

UNIT-V

Transients in Power Systems: Causes of over voltages. Travelling Wave Theory -Wave equation -Open Circuited Line -The short circuited line

junction of lines of different natural impedances- -Reflection and refraction Coefficients -Junction of Cable and overhead lines -Junction of three lines of different natural impedances -Bewley Lattice diagram.

Suggested Reading:

1. C.L. Wadhwa, *Electrical Power Systems,* Wiley Eastern Ltd., 4dtEdition, 2006.
2. John J. Grainger William D.Stevenson Jr. *Power System Analysis,* Tata McGraw Hill Edn. 2003
3. I.J. Nagrath & D.P.Kothari *Modern Power Systems Analysis,* TMH Edition, 2003.
4. A.Chakrabarti, M.L.Soni, P. V.Gupta, U.S.Bhatnagar, *A Text book on Power System,* Dhanpat Rai & Co (P) Ltd -1999.

EE 302

ELECTRICAL MACHINERY - II

Instruction	4/1	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Parallel operation of Single phase Transformer and load sharing. Insulation of Windings and terminals. Cooling arrangement in Transformers. Testing of Transformers -Routine Tests and Special tests -Measurement of Voltage ratio and check for voltage vector relationship. Measurement of No- load loss and current. Measurement of Insulation resistance. Maintenance of Transformers.

UNIT-II

Poly-phase Transformer Connections ,Choice of Transformer Connections, Third harmonic voltages -Phase Conversion -3phase to 2-phase transformation -Scott connection. Constructional features of three-phase transformers, tertiary winding, parallel operation of transformer, Auto Transformer -Comparison with two winding transformers- Conversion of two winding transformer to auto transformer. Tap changer on transformers, No-load tap changer, On-load tap changer.

UNIT-III

Three-phase Induction Motor -Constructional features –Rotating Magnetic field theory —Principle of operation of squirrel cage and slip ring motors -Vector Diagram , Equivalent circuit -Expression for torque- Starting torque, Maximum torque -Slip/Torque characteristics - Performance characteristics -Equivalent circuits from test –Current loci circle diagram - Predetermination of characteristics of Induction Motors .

UNIT-IV

Starting methods of Induction motors .Modes of operation, torque and power limits of Induction motors-Speed control methods -Resistance Control, Voltage control, pole changing, Cascading, variable frequency

control- Slip power recovery schemes Kramer drive. Scherbius drive-Double cage Induction motors. Induction generator

UNIT-V

Unbalanced Operation: Voltage Unbalance -Unbalanced Operation of 3-phase Induction Motor -Per Phase Equivalent Circuits -Single Phasing-Unbalanced Operation of 3-Phase Transformers –Single phase load on Three phase transformers Single Phasing in 3 phase transformers- Delta / Star and Star/Delta transformers.

Suggested Reading:

1. I.J. Nagarath, D.P.Kothari, *Electrical Machines*. 4th Edition Tata McGraw Hill, 2010.
2. J.B. Gupta, *Theory and Performance of Electrical Machines,* S.K. Kataria. & Sons, 2003.
3. P.S. Bimbhra, *Generalised theory of Electrical Machines,* Khanna Publishers Fifth Edition 1995
4. M.G.Say, *The performance and Design of A.C. Machines*- Pitman, 1985.
5. Fitzerald A E and Kingzley, *Electrical Machines,* .3rd Edition.

EE 303

POWER ELECTRONICS

(Common to IE & EEE)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Power Semiconductor Diodes and Transistors: Types of power diodes-General purpose diodes -Fast recovery diodes -Their characteristics and applications. Bipolar Junction transistors, Power MOSFETs P-Channel, N- Channel. IGBTs -Basic structure and working, Steady state and switching characteristics-Comparison of BJT, MOSFET and IGBT -Their applications. ISCRs-Static and dynamic characteristics,Two transistor analogy.

UNIT-II

Turn on and turn off mechanism of BJT , Power MOSFET, IGBTs .SCR trigger circuits-R, RC and UJT triggering circuits. Triggering circuits for Single phase bridge rectifier and Choppers. Driver Circuits for MOSFET, IGBT and BJT. The various commutation methods of SCRs. Protection of SCRs . GTO's - Basic structure, principle of operation, characterisics and applications.

UNIT-III

Principles of controlled rectification -Study of Single phase and three-phase half controlled and full controlled bridge rectifiers with R, RL, RLE loads. Effect of source inductances. Dual converters- circulating current mode and circulating current free mode-control strategies.

UNIT-IV

Classification of Choppers A, B, C, D and E, Switching mode regulators-Study of Buck, Boost and Buck-Boost regulators, Cuk regulators . Principle of operation of Single phase bridge type Cyclo converters and their applications. Single phase AC Voltage Controllers with R, and RL loads.

UNIT-V

Principle of operation of Single phase Inverters -Three phase bridge Inverters (180^0 and 120^0 modes)-voltage control of inverters-Single pulse width modulation- multiple pulse width modulation, sinusoidal pulse width modulation. Comparison of Voltage Source Inverters and Current source Inverters, Elementary Multilevel Inverters.

Suggested Reading:

1. Singh.M.D and Khanchandani.K.B,-*Power Electronics,* Tata McGraw Hill, 2nd Edition, 2006.
2. Rashid.M.H. *Power Electronics Circuits Devices and Applications.* Prentice Hall of India, 2003
3. M.S.Jamil Asghar, *Power Electronics,* Prentice Hall of India, 2004
4. Bimbra.P.S, *Power Electronics,* Third Edition, Khanna Publishers, 1999
5. Mohan, Undeland, Robbins, *Power Electronics,* John Wiley, 1996.

EE 304

DIGITAL ELECTRONICS AND LOGIC DESIGN

(Common to IE & EEE)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Boolean Algebra and combinational logic AND,OR and NOT operations, Laws of Boolean Algebra, minimization of Boolean expressions, Truth tables and maps sum of products and product of sums -map method of reduction, incompletely specified functions multiple output minimization.

UNIT-II

Tabular minimization, Digital logic families and IC's, Characteristics of Digital IC's, Introduction to RTL, DTL, TTL, CMOS, ECL families, Details of TTL logic family -totem pole, open collector outputs. Wired AND operation, comparison of performance, TTL subfamilies, multiplexer and de-multiplexer, encoder and decoder, code converters, implementation of combinational logic using standard logic gates and multiplexers.

UNIT-III

Binary arithmetic and circuits -Half and Full adder- subtractor and Magnitude comparator, number complements-two's complement arithmetic, carry look ahead adder, decimal numbers and their codes, BCD and Excess-3 arithmetic.

UNIT-IV

Synchronous Sequential Circuits -Basic latch circuit -debouncing switch - SR., JK, D and T flip-flops-truth table and excitation table -ripple and synchronous counters up/down counter -general BCD counter- Counter decoding-shift registers, ring counters.

UNIT-V

Design of Digital Systems -Concept of state. State diagram-design of counters Sequence detector and generators -Design procedure, synthesis using D, JK, T flip-flops -applications of registers -concepts of programmable logic -PROM, PLA, PAL.

Suggested Reading:

1. Donald Pleach / Albert Paul Malvino / Goutam Saha *"Digital Principles and Applications"* McGraw- Hill, 2006.
2. Tocci & Widmer, *Digital Systems*-Pearson Education-Eigth Edition, 2003.
3. Morris Mano M.., *Digital Design,* Prentice Hall of India, Third Edition, 2002.
4. B. Somnadh Nair, *Digital Electronics and Logic Design,* Prentice Hall, India, 2002.
5. Floyd, *Digital Fundamentals,* 4th edition, Universal Book Stall, New Delhi, 1992.
6. J.P. Uyemura, *A First Course in Digital Systems Design,* Brooks/ Cole Publishing Co., (Available from Vikas Publishing House in India).

EE 305

LINEAR INTEGRATED CIRCUITS

(Common to IE & EEE)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Operational amplifiers -Characteristics, open loop voltage gain, output impedance, input impedance, common mode rejection ratio -Offset balancing techniques -Slew rate, Frequency response -Stability, frequency compensation of Op-amp, basic applications -inverter summer, analog integrator, differentiator, current to voltage converter, voltage to current converter, voltage follower, ac amplifier.

UNIT-II

Voltage limiter, clipper and clamper, precision rectifier-full wave and half wave, peak detector, comparator, zero crossing detector, Schmitt trigger, monostable, astable, bistable multiplier, divider, difference amplifier instrumentation amplifier circuits using Op-amps.

UNIT-III

Waveform generation using Op-amps- Sine, Square, Triangular and Quadrature oscillators, voltage controlled oscillator / multi vibrator, voltage to frequency converter, 555 timer functional diagram, operation as monostable and astable. phase locked loop, A/D and D/ A converters.

UNIT-IV

Series voltage regulator using Op-amp, shunt regulators using Op-amp, switching regulators using Op-amp, dual voltage regulator ,fixed voltage regulators, dual tracking regulators ,hybrid regulator, current sensing and current feedback protection.

UNIT-V

RC active filters, low pass, high pass band pass, band reject, notch, first order, second order transformation, state variable filter, switched capacitor filter, universal filter. Balanced modulator/ demodulator.

Suggested Reading:

1. D.Roy Choudhury, *Linear Integrated Circuits,* Shail B.Jain, 3rd Edition, New Age International(P) Ltd., 2007.
2. Malvino Albert Paul, *Electronic Principles,* 7th Edition, Tata McGraw Hill, 2006
3. Coughlin and Driscoll, *Operational Amplifiers and Linear integrated Circuits,* 6th Edition, Prentice hall of India 2003.
4. David A. Bell, *Operational Amplifiers and Linear IC s,* PHI, 2003.
5. Gayakwad R.A. *Op-Amps and Linear Integrated Circuits,* 4th Edition, Prentice Hall of India, 2002.
6. S. Franco, *"Design with Operational Amplifiers and Analog Integrated Circuits",* McGraw Hill Inc., 2002 (Available from Tata McGraw Hill in India).

EE 306

LINEAR CONTROL SYSTEMS

(Common to IE & EEE)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Open and Closed loop Systems, Continuous time and discrete time control systems. Control system components, Error sensing devices, Potentiometers. Synchros, AC-DC servo motors-Block diagram representation, Transfer function and impulse response, Signal flow graphs.

UNIT-II

Time Response: Types of Input, Transient response of second order system for step input. Time domain specifications - Types of system- static error coefficients, Error Series-Routh-Hurwitz criterion of stability. Root Locus Technique- Typical systems analyzed by root locus technique-Effect of location of roots on system response PID Controller.

UNIT-III

Frequency Response Plots: Bode Plots, Frequency domain specifications. : Mp, w_p for a second order system, Nyquist criterion for a stability, relative stability, gain and phase margin, Compensation: Cascade Compensation using Bode plots.

UNIT-IV

State Space Representation: Concept of State, State Variable, State Models of linear time invariant systems. Derivation for state models from transfer functions and differential equations. State Transition matrix- Solution of State equations by time domain method. Observability and Controllability.

UNIT-V

Discrete Control Analysis: Introduction to signals and systems, The Z-transformation, digital control, advantages and disadvantages. Digital

control system architecture. The discrete transfer function. Sample data system. Transfer function of sample data systems- Z-plane specifications of control system design.Z-domain stability.

Suggested Reading:

1. I.J.Nagrath, M.Gopal, *Control System Engineering,* New Age International (P) Limited Publishers, 5th Edition, 2007.
2. J.F.Franklin and J.D.Powell, *Digital Control of Dynamic Systems,* Addison Wesley, 1980.
3. M.Gopal, *Control Systems Principles and Design*, Tata McGraw Hill, 2nd Edition, 2003.
4. K.Ogata, *Modern Control Systems,* 3rd Edition.PHI, 2000.
5. B.C. Kuo, *Automatic Control Systems,* 8th edition, Prentice Hall, New Delhi, 2002.
6. Shinners S.M., *Modern Control Engineering,* Prentice Hall, New Jersey, 1995.
7. D'azzo and Houpis, *Linear Control System Analysis and Design*, 4th edition, Singapore, 1995.

EE 331

ELECTRICAL MACHINES LAB - I

Instruction	3	Periods per week
Duration of University Examination	3	Hours
University Examination	50	Marks
Sessional	25	Marks

List of Experiments:

1. Magnetization characteristics and the speed Vs voltage curve of separately and self excited D.C. generator
2. Load characteristics of separately excited and Shunt Generators
3. Load characteristics of Compound generator
4. Performance characteristics of Series Motor
5. Performance characteristics of D.C. shunt motor
6. Performance characteristics of Compound motor
7. Separation of iron and friction losses and estimation of parameters in D.C. machines.
8. (a) Speed control of D.C. shunt motor by shunt field control and armature resistance control (b) Swinbum's Test
9. Separation of core losses in a Single Phase transformer
10. Open circuit and short circuit tests on a Single Phase transformer
11. Sumpner's test on two identical transformers
12. Estimation of efficiency of DC Machine by Hopkinson test.

Note : Atleast 10 experiments should be conducted in the Semester.

EE 332

CONTROL SYSTEMS LAB

(Common to IE & EEE)

Instruction	3	Periods per week
Duration of University Examination	3	Hours
University Examination	50	Marks
Sessional	25	Marks

List of Experiments:

1. Characteristics of D.C. and A.C. Servo motors.
2. Characteristics of Synchro Pair.
3. Frequency response of compensating networks.
4. Step response of second order system.
5. D.C.Positon Control System.
6. A.C.position Control System.
7. Closed loop P, PI and PID Controller.
8. Step response and Frequency response of a given plant.
9. Design of lag and lead compensation for the given plant.
10. ON/OFF Temperature Control systems.
11. Temperature control system.
12. Level Control system

Note : Atleast 10 experiments should be conducted in the Semester.

SCHEME OF INSTRUCTION & EXAMINATION

B.E. IIIrd YEAR

(ELECTRICAL AND ELECTRONICS ENGINEERING)

SEMESTER - II

Sl. No.	Syllabus Ref. No.	SUBJECT	Scheme of Instruction		Scheme of Examination		
			Periods per week		Duration In Hours	Maximum Marks	
			L/T	D/P		Univ. Exam	Sessionals
		THEORY					
1.	EE 351	Digital Signal Processing	4	-	3	75	25
2.	EE 352	Electrical Machinery - III	4/1	-	3	75	25
3.	EE 353	Switchgear and Protection	4	-	3	75	25
4.	EE 354	Microprocessor and Microcontrollers	4	-	3	75	25
5.	CM 371	Managerial Economics and Accountancy	4	-	3	75	25
		PRACTICALS					
1.	EE 381	Electrical Machines Lab-II	-	3	3	50	25
2.	EE 382	Power Electronics Lab	-	3	3	50	25
3.	EE 383	Integrated Circuits Lab	-	3	3	50	25
4.	EE 384	Industrial Visit	-	-	-	-	*Gr
		Total	**20/1**	**9**	**24**	**525**	**200**

**Excellent / Very Good / Good / Satisfactory / Unsatisfactory*