SCHEME OF INSTRUCTION & EXAMINATION

B.E. IInd YEAR
INFORMATION TECHNOLOGY

SEMESTER - I

Sl. No.	Syllabus Ref. No.	SUBJECT	Scheme of Instruction		Scheme of Examination		
			Periods per week		Duration In Hours	Maximum Marks	
			L	D/P		Univ. Exam	Sessionals
		THEORY					
1.	BIT 201	Discrete Mathematics	4	-	3	75	25
2.	BIT 202	Microelectronics	4	-	3	75	25
3.	BIT 203	Digital Electronics & Logic Design	4	-	3	75	25
4.	BIT 204	Data Structures	4	-	3	75	25
5.	EE 223	Electrical Circuits & Machines	4	-	3	75	25
6.	CE 222	Environmental Studies	4	-	3	75	25
		PRACTICALS					
1.	BIT 231	Basic Electronics - Lab	-	3	3	50	25
2.	BIT 232	Data Structures - Lab	-	3	3	50	25
3.	BIT 233	Mni Project - I	-	3	-	-	25
		TOTAL	**24**	**9**	**-**	**550**	**225**

WITH EFFECT FROM THE ACADEMIC YEAR 2011 - 2012

BIT 201

DISCRETE MATHEMATICS

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Logic - Sets and Functions : Logic, Propositional equivalences - Predicates and quantifiers - Nested quantifiers-Sets-Set Operations, Functions.

Algorithms-Integers-Matrices : Algorithms, Complexity of Algorithms. The Integers and Division, integers and Algorithms, Applications of Number Theory, Matrices.

UNIT-II

Mathematical Reasoning, Induction, and Recursion: Proof Strategy, Sequence and Summation, Mathematical Induction, Recursive Definitions and Structural Induction, Recursive Algorithms.

Counting - Basics, pigeonhole principle, Permutations and combinations-Binomial Coefficients, Generalized Permutations and combinations, Generating permutations and combinations.

UNIT-III

Discrete Probability : An Introduction to Discrete Probability, Probability theory, Expected Value and Variance.

Advances Counting Techniques : Recurrence relations - Solving Recurrence Relations - Divide and conquer relations - and Recurrence Relations, Generating function-Inclusion - Exclusion-Applications of Inclusion-Exclusion.

UNIT-IV

Relations : Relations & their Properties, n-ary relations and applications, Representing relations-Closures, equivalence relations, partial orderings.

Graphs : Introduction, Graph terminology, representing Graphs and Graph Isomorphism, Connectivity, Euler and Hamiltonian paths, Shortest path problems, Planar graphs, Graph coloring.

UNIT-V

Trees : Introduction to Trees, Application of Trees, Tree Traversal, Spanning Trees, Minimum Spanning Trees.

Boolean Algebra : Boolean function, Representing Boolean Functions, Logic Gates, Minimization of Circuits.

Suggested Reading :

1. Kenneth H. Roen-Discrete *Mathematics and its application*- 5th edition, McGraw-Hill, 2003.
2. J.K. Sharma, *Discrete Mathematics,* Second edition, Macmillan, 2005.
3. J.P. Trembly, R. Manohar, *Discrete Mathematical Structure with Application to Computer Science,* McGraw-Hill, 1997.
4. Joel. Mott. Abraham Kandel, P.P. Baker, *Discrete Mathematics for computer Scientist & Mathematicians,* Prentice Hail N.J. 2nd edn, 1986.

BIT 202

MICRO ELECTRONICS

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT – I

Semi-conductors, Conductors, and Insulators, Covalent bonds, conduction in semi-conductors, N-type and P-type semi-conductors, PN junction, Biasing, Zener diodes, Rectifier Circuits, Limiting and clamping circuits, Schottky Barrier diode and Varactor diode.Cathode Ray Oscilloscope and its applications

UNIT – II

Bipolar junction transistors – Physical structure and modes of operation, npn transistor, pnp transistor, characteristics, analysis of transistor circuits at DC, transistor as amplifier, small signal equivalent circuit models, biasing, transistor as switch, internal capacitance.

MOSFET current-voltage characteristics, MOSFET as an amplifier and as a switch, biasing, Internal capacitance.

The Junction Field-Effect Transistors(JFET) – Structure and physical operation, characteristics.

UNIT – III

Feedback – Structure, Properties of negative feedback, Topologies, Advantages of negative feedback. Sinusoidal Oscillators – Loop gain, Barkhausen criteria, RC Phase shift, LC and Crystal Oscillators.
Power Amplifiers: class A, B and C amplifiers.

UNIT – IV

Operational Amplifiers : Ideal characteristics, op. amp. as adder, Subtractor, Integrator, differentiator and comparator using op. amp. generation of square and Triangular waveforms, Monostable multi vibrator.

Op. Amp. As Voltage –controlled current switch(VCCS), Current-controlled Voltage source(CCVS), Instrumentation Amplifier, antilogarithmic amplifiers and analog multipliers.

UNIT – V

Digital CMOS logic circuits: Introduction, digital IC technologies and logic circuit families, Voltage Transfer Characteristic (VTC) of inverter, Noise Margins, Propagation delay, static and dynamic operation of CMOS inverter. CMOS logic gate circuits: Basic structure (PUN and PDN), Implementation of 2-input NOR gate, NAND gate, complex gates and exclusive OR gate.

Suggested Reading :

1. Adel S. Sedra, Kenneth C. Smith, *Micro Electronic Circuits,* 5th Edition, Oxford International Student Edition, 2006
2. Jocob Millman, Arvin grable, *Micro Electronics,* 2nd Edition, McGraw Hill 1987.
3. Shilling, L.D., Belove, C., *Electronic Circuit – Discrete Integrate,* 3rd Edition, McGraw Hill, ISE, 1989.

BIT 203

DIGITAL ELECTRONICS & LOGIC DESIGN

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT – I

Design Concepts – Digital Hardware, Design process, Design of digital hardware Introduction to logic circuits – Variables and functions, Logic gates and networks. Boolean algebra, Synthesis using gates, Design examples. Optimized implementation of logic functions – Karnaugh Map, Strategies for minimization minimizing product-of-sum functions. Multiple output circuits. NAND and NOR logic networks Introduction to CAD tools and VHDL

UNIT – II

Programmable logic devices: geneal structure of a PLA, gate level diagram, schematic diagram, PAL. Structure of CPLDs and FPGAs, 2-input and 3-input lookup tables(LUT). Design of Arithmetic-circuits using CAD tools. Combinational circuit building blocks – Multi-plexers. Decoders. Encoders. Code converters, Arithmetic comparison circuits. VHDL for Combinational circuits

UNIT – III

Basic Latch, Gated SR Latch, gated D Latch Master-Slave edge triggered flip-flops. T Flip-flop, JK Flip-flop, excitation tables. Registers, Counter. Using registers and counters with CAD tools. Design examples using VHDL.

UNIT – IV

Synchronous Sequential Circuits – Basic design steps. State-Assignment problem Moore and Mealy state mode. Design of Finite state machines with CAD tools, example. State minimization, FSM as an Arbiter Circuit, Analysis of Synchronous sequential Circuits. Algorithmic State Machine carts, formal model.

Implementation using VHDL.

UNIT – V

Asynchronous Sequential Circuits – Behavior, Analysis, Synthesis, State reduction, State Assignment, examples.

Hazards : static and dynamic hazards. Significance of Hazards.
Clock skew, set up and hold time of a flip-flop, Shift and add multiplier, data path circuit for the multiplier, ASM chart and datapath circuit for the divider control circuit, sort operation.

Implementation using VHDL code.

Suggested Reading:

1. Stephen Brown Zvonko Vranesic, *Fundamentals of Digital Logic with VHDL design,* McGraw Hill, 2000.
2. Enocho Hwang, *Digital Logic and Microprocessor Design with VHDL,* Thomson, 2006.
3. John F. Wakerly, *Digital design Principles & Practices,* 3rd Edition, Prentice Hall.
4. M. Moris Mano, Charles R. Kime, *Logic and Computer Design Fundamentals,* 2nd edition, Pearson Education Asia, 2001.
5. H.T. Nagle, *Introduction to Computer Logic,* Prentice Hall, 1975.

BIT 204

DATA STRUCTURES

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT - I

Algorithm Specification, Performance Analysis and Measurement.

Arrays: Abstract Data Types and the C++ Class, Array as an Abstract Data Type, Polynomial Abstract Data Type, Sparse Matrices, Representation of Arrays, String Abstract Data Type.

UNIT - II

Stacks and Queues: Templates in C++, Stack Abstract Data Type, Queue Abstract Data type, Subtyping and Inheritance in C++, A Mazing Problem, Evaluation of Expressions.

UNIT - III

Linked Lists: Singly Linked Lists and Chains, Representing Chains in C++, Template Class Chain, Circular Lists, Available Space Lists, Linked Stacks and Queues, Polynomials, Doubly Linked Lists.

Hashing: Static Hashing, Hash Tables, Hash Functions, Secure Hash Functions, Overflow Handling, Theoretical Evaluation of Overflow Techniques

UNIT - IV

Trees: Introduction, Binary Trees, Binary Tree Traversal and Tree Iterators, Copying Binary Trees, Threaded Binary Trees, Heaps, Binary Search Trees.
Graphs: Graph Abstract Data Type, Elementary Graph operations (dfs and bfs), Minimum Cost Spanning Trees (Prim's and Kruskal's Algorithms).

UNIT - V

Sorting: Insertion sort, Quick sort, Best computing time for Sorting, Merge sort, Heap sort, Sorting on Several Keys, List and Table Sorts, Summary of Internal Sorting.

Efficient Binary Search Trees: AVL Trees, Red-Black Trees, Splay Trees, m-way Search Trees, B-Trees.

Suggested Reading:

1. Ellis Horowitz, Dinesh Mehta, S. Sahani. *Fundamentals of Data Structures in C++,* Universities Press. 2007.
2. Mark Allen Weiss, *Data Structures and Algorithm Analysis in C++,* Pearson Education 2006.
3. Michael T. Goodrich, Roberto Tamassia, David Mount, *Data structures and Algorithms in C++,* Wiley India Pvt. Ltd, 2004

EE 223

ELECTRICAL CIRCUITS AND MACHINES

(Common for Mechanical Engineering & IT Branches)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT – I

DC Circuits: Ohm's Law, Network elements, Kirchoff's Law, Power in DC circuits, Series and parallel resistances, Thevinin's and Norton's theorems.

AC Circuits: Sinusoidal sources, Phasor representation of sinusoidal quantities, Average and RMS values, Form factor, Analysis of RLC Circuits to sinusoidal inputs, Power factor, Active & reactive powers, energy stored in inductance and capacitance, Mutual inductance.

UNIT – II

Three-Phase Voltages: Production of 3-phase voltages, balanced star and delta connections, Measurement of power by Two-wattmeter method.

Single Phase Transformers: Principle of operation, Transformer on No-load and Load, Equivalent circuit, Efficiency & regulation, O.C and S.C tests, Principal of Autotransformer

UNIT – III

DC machines: Construction and working principle, EMF in Generator, types of excitation, characteristics of series and Shunt generators, Applications, Torque in a DC motor, Characteristic of Shunt and Series motors, Speed control of DC shunt motors, losses and efficiency, three point starter.

UNIT – IV

Three Phase Introduction Motors: Production of rotating magnetic field, construction and principle of induction motors, Torque –slip characteristics, Star delta and Auto-transformer starters, Speed control by Stator voltage and Rotor resistance methods.

UNIT – V

Single Phase Motors: Capacitor start and Capacitor run motor, Stepper motor.

Three Phase Alternators: Construction, production of EMF, Regulation by synchronous impedance method.

Suggested Reading:

1. M.S. Naidu and Kamakshaiah, *Introduction to Electrical Engineering,* Tata McGraw Hill, 1995.
2. V.K. Mehta, *Principles of Electrical Engineering and Electronics,* S. Chand & Co, 1995.
3. Cotton H., *Electrical Technology,* BI Publications, 1985

CE 222

ENVIRONMENTAL STUDIES

(Common to all Branches)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNI-I

Environmental studies: Definition, scope and importance, need for public awareness. Natural resources: Water resources; use and over utilization of surface and ground water, floods, drought, conflicts over water, dams benefits and problems. Effects of modern agriculture, fertilizer-pesticide problems, water logging salinity. Energy resources, growing energy needs, renewable and non-renewable energy sources. Land Resources, land as a resource, land degradation, soil erosion and desertification.

UNIT-II

Ecosystems: Concepts of an ecosystem, structure and functions of an ecosystem, producers, consumers and decomposers, energy flow in ecosystem, food chains, ecological pyramids, aquatic ecosystem (ponds, streams, lakes, rivers, oceans, estuaries).

UNIT-III

Biodiversity: Genetic species and ecosystem diversity, bio-geographical classification of India. Value of biodiversity, threats to biodiversity, endangered and endemic species of India, conservation of biodiversity.

UNIT-IV

Environmental Pollution: Causes, effects and control measures of air pollution, water pollution, soil pollution, noise pollution, thermal pollution and solid waste management.

Environment Protection Act: Air, water, forest and wild life acts, issues involved in enforcement of environmental legislation.

UNIT-V

Social Aspects and the Environment: Water conservation, watershed management, and environmental ethics. Climate change, global warming,

acid rain, ozone layer depletion. Environmental protection act, population explosion.

Disaster Management: Types of disasters, impact of disasters on environment, infrastructure and development. Basic principles of disaster mitigation, disaster management, and methodology, disaster management cycle, and disaster management in India.

Suggested Reading :

1. A. K. De, *Environmental Chemistry*, New Age Publications, 2002.
2. E. P. Odum, *Fundamentals of Ecology*, W.B. Sunders Co., USA.
3. GL. Karia and R.A. Christian, *Waste Water Treatment, Concepts and Design Approach*, Prentice Hall of India, 2005.
4. Benny Joseph, *Environmental Studies*,TataMcGraw-Hill, 2005
5. V. K. Sharma, *Disaster Management*, National Centre for Disaster Management, IIPE, Delhi, 1999.

BIT 231

BASIC ELECTRONICS LABORATORY

Instruction	3	Periods per week
Duration of University Examination	3	Hours
University Examination	50	Marks
Sessional	25	Marks

ANALOG:

1. CRO and its applications: Measurement of amplitude, frequency. Obtaining transfer characteristics and lissajous figures. Determination of unknown frequency using CRO.
2. Characteristics of pn junction diode , zener diode, BJT and FET. Applications: Half-wave and full-wave rectifiers, clipping and clamping circuits, BJT and FET as switches
3. Frequency response of Common Emitter amplifier
4. Hartley, colpitts and RC phase shift oscillators
5. Operational Amplifier as an adder, subtractor, differentiator, integrator and comparator

DIGITAL:

6. Truth table verification of logic gates using TTL 74 series ICs. Transfer characteristics of a TTL gate using CRO
7. Half Adder, Full Adder, Decoder, MUX, implementation of Boolean logic using decoders and MUXes.
8. Truth table verification of D flip flop, T flip-flop and JK flip-flop
9. Counters
10. Shift Registers

SOFTWARE:

Any 3 experiments using PSPICE.

Note : All the experiments are compulsory.

BIT 232

DATA STRUCTURES LABORATORY

Instruction	3	Periods per week
Duration of University Examination	3	Hours
University Examination	50	Marks
Sessional	25	Marks

List of Experiments:

1. Implementation of array ADT
2. Implementation of String ADT
3. Implementation of Stacks, Queues.
4. Infix to Postfix Conversion, evaluation of postfix expression.
5. Polynomial arithmetic using linked list.
6. Implementation of Binary Search and Hashing.
7. Implementation of Selection, Shell, Merge and Quick sorts.
8. Implementation of Tree Traversals on Binary Trees.
9. Implementation of Heap Sort.
10. Implementation of operations on AVL Trees.
11. Implementation of Traversal on Graphs.
12. Implementation of Splay Trees.

BIT 233

MINI PROJECT - I

Instruction	3	Periods per week
Sessional	25	Marks

The Students are required to implement one of the projects from project exercise given in the suggested readings of the theory subjects. During the implementation of the project, Personnel Software Process (PSP) has to be followed. Report of the projectwork has to be submitted for evaluation.