SCHEME OF INSTRUCTION & EXAMINATION

B.E. IV - YEAR
(INFORMATION TECHNOLOGY)

SEMESTER - I

Sl. No.	Syllabus Ref. No.	SUBJECT	Scheme of Instruction		Scheme of Examination		
			Periods per week		Duration In Hours	Maximum Marks	
			L	D/P		Univ. Exam	Sessionals
		THEORY					
1.	BIT 401	VLSI Design	4	-	3	75	25
2.	BIT 402	Middleware Technologies	4	-	3	75	25
3.	BIT 403	Information Security	4	-	3	75	25
4.		ELECTIVE-II	4	-	3	75	25
5.		ELECTIVE-III	4	-	3	75	25
		PRACTICALS					
1.	BIT 431	VLSI Design Lab	-	3	3	50	25
2.	BIT 432	Middleware Technologies Lab	-	3	3	50	25
3.	BIT 433	Project Seminar	-	3	-	-	25
		Total	**20**	**9**		**475**	**200**

Elective-II

BIT 404 Wireless and Mobile Communications
BIT 405 Ad-hoc and Sensor Networks
BIT 406 Distributed Systems
LA 473 Intellectual Property Rights

Elective-III

BIT 408 Digital Image Processing
BIT 409 Grid Computing
BIT 410 CPLD and FPGA Architecture
BIT 411 Software Reuse Techniques
BIT 412 Semantic Web

WITH EFFECT FROM THE ACADEMIC YEAR 2013 - 2014

BIT 401

VLSI DESIGN

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

An overview of VLSI, Moore's law, Electrical Conduction in Silicon, Electrical Characteristics of MOSFETs Threshold voltage, nFET Current-Voltage equations, square law and linear model of a FET, MOS capacitances, gate-source and gate drain capacitances, junction capacitances in a MOSFET, RC model of a FET, modeling small MOSFET, scaling. MOSFET as switches, pass characteristics, logic gates using CMOS, Bubble pushing, XOR and XNOR gates, AOI and OAI logic gates, transmission gates. TG based 2-to-1 MUX, XOR, XNOR, OR circuits.

UNIT-II

Physical structure of CMOS ICs, IC layers, layers used to create a MOSFET, Top and side view of MOSFETs, Silicon patterning or layouts for series and parallel connected FETs. Layouts of NOT gate, transmission gate, noninverting buffer, NAND2, NOR2, Complex logic gate, 4 input AOI gate. Stick diagram representations. Layouts of Basic Structure: nwells, active area definition, design of n^+, p^+ regions, masks for the nFET, active contact cross section and mask set, metal1 line with active contact, poly contact: cross section and layout, vias and higher level metals. Latchup prevention.

UNIT-III

Fabrication of CMOS ICs, CMOS process flow, Design rules: minimum space width, minimum spacing, surround, extension, cell concepts and cell based design, logic gates as basic cells, creation of new cell using basic gates. DC characteristics of the CMOS inverter symmetrical inverter, layouts, Inverter switching characteristics, RC switch model equivalent for the CMOS inverter, fanout, input capacitance and load effects, rise time and fall time calculation, propagation delay, driving large capacitive loads, delay minimization in an inverter cascade.

UNIT-IV

Pseudo nMOS, tristate inverter circuits, chocked CMOS, charge leakage, Dynamic CMOS logic circuits, precharge and evaluation charge sharing, Domino logic, Dual rail logic networks, differential Cascade Voltage Switch Logic (CVSL) AND/NAND, OR/NOR gates, Complementary Pass Transister Logic (CPL). The SRAM, 6T SRAM cell design parameters, writing to an SRAM, resistor model, SRAM cell layout, multi port SRAM, SRAM arrays, Dynamic RAMs: 1T RAM cell, charge leakage and refresh in a DRAM cell, physical design of DRAM cells. NOR based ROM, ROM array using pseudo nMOS circuitry, floating gate MOSFET, effect of charge storage on the floating gate, A E^2PROM word using floating gate nFETs, logic gate diagram of the PLA, NOR based design, CMOS PLA, Gate arrays.

UNIT-V

VLSI Design flow, structural gate level modeling, gate primitives, gate delays, switch level modeling, behavioral and RTL operators, timing controls, blocking and non blocking assignments, conditional statements, Data flow modeling and RTL, Comparator and priority encoder barrel shifter, D latch Master slave D type flip-flop, Arithmetic circuits; half adder, full adder, AOI based, TG based, ripple carry adders, carry look ahead adders, High speed adders, multipliers. Interconnect modeling; Interconnect resistance and capacitance sheet resistance Rs, time delay, single and multiple rung ladder circuits, simple RC inter connect model, modeling inter connect lines with a series pass FET, cross talk, floor planning and routing, clocking, Testing of VLSI circuits.

Suggested Reading:

1) John P. Uyemura, *"Introduction to VLSI circuits and Systems"*, John Wiley & Sons, 2002
2) John P. Uyemura, *"Chip design for submicron VLSI: CMOS layout and simulation"* IE, Cengage learning, 2006.
3) Douglas A. Pucknell, Kamran Eshraghian, *"Basic VLSI Design"* 3rd Edition, PHI, 2000.
4) Jan M. Rabey and others *"Digital Integrated Circuits A design perspective"*, Pearson Education.

BIT 402

MIDDLEWARE TECHNOLOGIES

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

CLIENT/SERVER CONCEPTS: Client – Server – File Server, Database server, Group server, Object server, Web server. Middleware – General middleware – Service specific middleware. Client/Server Building blocks – RPC – Messaging – Peer – to – Peer. Web Services- SOA, SOAP, WSDL, REST Services

UNIT-II

SERVLETS: Servlet Lifecycle, sending HTML information, Session tracking, JDBC API, Applications.

STRUTS: An introduction to Struts Framework, Basic components of struts, Model Layer, view Layer, Controller Layer, and Validator.

UNIT-III

EJB ARCHITECTURE: EJB –EJB Architecture – Overview of EJB software architecture – View of EJB – Conversation – Building and Deploying EJBs – Roles in EJB.

EJB APPLICATIONS: EJB Session Beans – EJB entity beans – EJB clients – EJB Deployment – Building an application with EJB.

UNIT-IV

CORBA: CORBA – Distributed Systems – Purpose – Exploring CORBA alternatives – Architecture overview – CORBA and networking model – CORBA object model – IDL – ORB – Building an application with CORBA.

UNIT-V

COM: COM – Data types – Interfaces – Proxy and stub – Marshalling – Implementing server/Client – Interface pointers – Object Creation, Invocation, Destruction – Comparison COM and CORBA – Introduction to .NET – Overview of .NET architecture–Marshalling – Remoting

Suggested Reading:

1) Robert Orfali, Dan Harkey and Jeri Edwards, "The Essential Client/ server Survival Guide", Galgotia publications Pvt. Ltd., 2002.(Unit 1)
2) Tom Valesky, "Enterprise Java Beans", Pearson Education, 2002.(Unit 2 & 3)
3) Jason Pritchard. "COM and CORBA side by side", Addison Wesley,2000 (Unit 4 & 5)
4) Jesse Liberty, "Programming C#", 2nd Edition, O'Reilly press,2002. (Unit 5)
5) Struts: the complete reference By James Holmes Edition: 2, illustrated Published by McGraw-Hill Professional, 2006(added)(unit-2)
6) Java Servlet Programming By Jason Hunter, William Crawford Edition: 2, illustrated Published by O'Reilly, 2001(unit-2)(added)
7) Arno Puder, kay Romere and Frank pilhofer. Distributed Systems Architecture, Morgan Kaufman 2006
8) Mowbray, " Inside CORBA", Pearson Education, 2002.
9) Jeremy Rosenberger, "Teach yourself CORBA in 14 days", Tec media,2000

BIT 403

INFORMATION SECURITY

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT- I

Introduction: History, critical characteristics of information, NSTISSC security model, Components of an information system, Securing the components, balancing security and access, The SDLC, The security SDLC

Need for Security: Business needs, Threats, Attacks-secure software development

UNIT-II

Legal, Ethical and Professional Issues: Law and ethics in information security, relevant U.S laws-international laws and legal bodies, Ethics and information security

Risk Management: Overview, Risk Identification, risk assessment, Risk Control strategies, selecting a risk control strategy, Quantitative versus qualitative risk control practices, Risk management discussion points, recommended risk control practices

UNIT-III

Planning for Security: Security policy, Standards and practices, Security blue print, Security education, Continuity strategies.

Security Technology: Firewalls and VPNs: Physical design, firewalls, protecting remote connections.

UNIT-IV

Security Technology: Intrusion detection, Access control and other security tools: Intrusion detection and prevention systems, Scanning and analysis tools, Access control devices.

Cryptography: Foundations of cryptology, cipher methods, crypryptographic Algorithms, Cryptographic tools, Protocols for secure communications, Attacks on cryptosystems

UNIT-V

Implementing Information Security: information security project management, technical topics of implementation , Non- technical aspects of implementation, Security certification and accreditation

Security and Personnel: Positioning and staffing security function, Employment policies and practices, internal control strategies.

Information security Maintenance: Security management models. The maintenance model, Digital forensics

Suggesting Reading :

1. Michael E. Whitman and Hebert J Mattord, Principles of Information Security, 4th edition Ed. Cengage Learning 2011.
2. Thomas R Peltier, Justing Peltier, John Blackley, Information Security. Fundamentals, Auerbacj Publications 2010.
3. Detmar W Straub, Seymor Goodman, Richard L Baskerville, Information Security. Policy proceses and practices PHI 2008.
4. Marks Merkow and Jim Breithaupt, Information Security. Principle and Practices, Pearson Education, 2007.

BIT 404

WIRELESS AND MOBILE COMMUNICATIONS (ELECTIVE –II)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Introduction to Wireless Communication Systems: Evolution of Mobile Radio Communications,

Examples of Wireless Communication Systems. Modern Wireless Communication Systems : Second Generation (2G) Cellular Networks, Third Generation (3G) Wireless Networks, Wireless local Loop, Wireless Local Area Networks.The Cellular Concept: Introduction, Frequency Reuse, Channel Assignment Strategies, Handoff Strategies, Interference and Systems Capacity, Trunking and Grade of Service, Improving Coverage & Capacity in Cellular Systems.

UNIT-II

Mobile Radio Propagation : Large Scale - :Path Loss : Introduction to Radio Wave Propagation, Free Space Propagation Model, Three Basic Propagation Mechanisms, Reflection, Ground Reflection, Diffraction, Scattering, Outdoor Propagation Models, Indoor Propagation Models, Signal Penetration into Buildings.

UNIT-III

Modulation Techniques for Mobile Radio : Digital Modulation, Linear Modulation Techniques, Constant Envelop Modulation, Spread Spectrum Modulation Techniques.

UNIT-IV

Multiple Access Techniques for Wireless Communications : FDMA, TDMA, Spread Spectrum Multiple Access, Space Division Multiple Access, Capacity of Cellular Systems. Wireless Networking : Introduction, Difference between Wireless and Fixed Telephone Networks, Development of Wireless Networks. Wireless Systems and Standards: Global System for Mobile (GSM), GPRS, CDMA Digital Cellular Standard.

UNIT-V

Mobile Network Layer: Mobile IP : Goals & Requirements, Terminology, IP Packet Delivery, Agent Advertisement & Discovery, Registration, Tunneling and Encapsulation, Optimizations, Reverse Tunneling. Dynamic Host Configuration protocol. Mobile Transport Layer: Traditional TCP, Snooping TCP, Mobile TCP, Fast Retransmit/Fast Recovery, Transmission/ Time-Out Freezing, Selective retransmission, Transaction oriented TCP

Suggested Reading:

1) Theodore S. Rappaport, "Wireless Communications Principles and Practice", 2nd Edition, Pearson Education, 2003.
2) Jochen Schiller, "Mobile Communication", 2nd Edition, Pearson Education.

BIT 405

AD-HOC AND SENSOR NETWORKS (ELECTIVE-II)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Wireless Transmission Technology and Systems: Introduction, Radio Technology Primer, Available Wireless Technologies. Medium Access Control Protocols for Wireless Networks:

Introduction, Background, Fundamentals of MAC Protocols.

UNIT-II

Adhoc Networks: Introduction and Definitions, Adhoc Network Applications, Design Challenges. Evaluating Adhoc Network Protocols - the Case for a Test bed. Routing in Mobile Adhoc Networks: Introduction, Flooding. Proactive Routing. On Demand Routing. Proactive Versus On Demand Debate. Location based Routing.

UNIT-III

Multicasting in Adhoc Networks: Introduction, Classifications of Protocols, Multicasting Protocols, Broadcasting. Protocol Comparisons, Overarching Issues. Transport layer Protocols in Adhoc Networks: Introduction, TCP and Adhoc Networks, Transport Layer for Adhoc Networks: Overview, Modified TCP, TCP-aware Cross-Layered Solutions. Adhoc Transport Protocol.

UNIT-IV

QoS Issue in Adhoc Networks: Introduction, Definition of QoS, Medium Access Layer, Q0S Routing, Inter- Layer Design Approaches. Security in Mobile Adhoc Networks: Vulnerabilities of Mobile Adhoc Networks, Potential Attacks, Attack Prevention Techniques. Intrusion Detection Techniques.

UNIT-V

Basic Wireless Sensor Technology: Introduction, Sensor Node Technology, Sensor Taxonomy.

Introduction and Overview of Wireless Sensor Networks: Introduction, Overview MAC Protocols for Wireless Sensor networks. Applications of Wireless Sensor Networks: Examples of Category 1 and Category 2 WSN applications.

Suggested Reading:

1) Prasant Mohapatra and Srihanamurthy, "Ad Hoc Networks Technologies and Protocols", Springer, Springer International Edition, 2009.
2) Kazem Sohraby, Daniel Minoli, Taieb Znati, "Wireless Sensor Networks", A John Wiley & Sons, Inc., Publication-2007.
3) Shivaram Murthy and B. S. Manoj, "Adhoc Networks – Principles and Protocols", Pearson Education, 2012.

BIT 406

DISTRIBUTED SYSTEMS (ELECTIVE –II)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Introduction: Definition of Distributed Systems, Goals: Connecting Users and Resources, Transparency, Openness, Scalability, Hardware Concepts: Multiprocessors, Homogeneous Multicomputer systems, Heterogeneous Multicomputer systems, Software Concepts: Distributed Operating Systems, Network Operating Systems, Middleware, The client-server model: Clients and Servers, Application Layering, Client-Server Architectures.

UNIT-II

Communication:Layered Protocols, Lower-Level Protocols, Transport Protocols, Higher-Level Protocols, Remote Procedure Call: Basic RPC Operation, Parameter Passing. Extended RPC Models, Remote Object Invocation: Distributed Objects, Binding a Client to an Object; Static verses Dynamic Remote Method Invocations, Parameter Passing, Message Oriented.

Communication: Persistence and synchronicity in Communication, Message-Oriented Transient Communication, Message-Oriented' Persistent Communication, Stream Oriented Communication: Support for Continuous Media, Streams and Quality of Service, Stream Synchronization.

UNIT-III

Process: Threads: Introduction to Threads, Threads in Distributed Systems, Clients: user Interfaces, Client-Side Software for Distribution Transparency, Servers: General Design Issues, Object Servers, Software Agents: Software Agents in Distributed Systems, Agent Technology, Naming: Naming Entities: Names, Identifiers, and Address, Name Resolution, The Implementation of a Name System, Locating Mobile Entities: Naming verses Locating Entities, Simple Solutions, Home-Based Approaches, Hierarchical Approaches.

UNIT-IV

Distributed Object based Systems: CORBA: Overview of CORBA, Communication, Processes, Naming, Synchronization, Caching and Replication, Fault Tolerance, Security, Distributed COM: Overview of DCOM, Communication, Processes, Naming, Synchronization, Replication, Fault Tolerance, Security, GLOBE: Overview of GLOBE, Communication, Process, Naming, Synchronization, Replication, Fault Tolerance, Security, Comparison of COREA, DCOM, and Globe: Philosophy. Communication. Processes. Naming. Synchronization. Caching and Replication, Fault Tolerance. Security.

UNIT-V

Distributed Multimedia Systems: Introduction. Characteristics of Multimedia Data. Quality of Service Management: Quality of Service negotiation. Admission Control. Resource Management: Resource Scheduling.

Suggested Reading:

1) Andrew S. Tanenbaum and Van Steen "Distributed Systems" . PHI, 2nd Edition.
2) Colouris G.. Dollimore Jean, Kindberg Tim, "Distributed Systems Concepts and Design". 3rd Edition Pearson education 2002.

LA 473

INTELLECTUAL PROPERTY RIGHTS (ELECTIVE-II)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Introduction: Meaning of Intellectual Property- Nature of I.P- Protection of I.P. Rights-kinds of Intellectual Property Rights –International Conventions of Intellectual Property Rights- patent Treaty 1970, GATT 1994, TRIPS & TRIMS – International Organization for Protection of IPR – WTO, WIPRO, UNESCO.

UNIT-II

Patents: Meaning of Patent- Commercial Significance – Obtaining of Patent – patentable Subject – matter – rights and obligations of Patentee – specification – Registration of patents – Compulsory licensing and licenses of rights – Revocation.

UNIT-III

Industrial Designs : Definitions of Designs – Registration of Designs – Rights and Duties of Proprietor of Design – Piracy of Registered Designs.

UNIT-IV

Trade Marks : Meaning of trademark – purpose of protecting trademarks Registered trade mark – procedure – passing off – Assignment and licensing of trademarks – Infringement of trademarks.

UNIT-V

Nature, scope of copyright – Subject matter of copy right – Right conferred by copyrightPublication – Broad – casting, telecasting – computer programme – Database right – Assignment – Transmission of copyright – Infringement of copy right.

Suggested Reading:

1) Cornish W.R, "Intellectual Property Patents", Copyright, Trademarks and Allied Rights, Sweet & Maxwell 1993.
2) P . Narayanan, "Intellectual Property Law", Eastern law House 2nd Edn. 1997.
3) Robin Jacob & Daniel Alexander, "A Guide Book to Intellectual Property Patents, Trademarks, Copy rights and designs", Sweet and Maxwell, 4th Edn.,1993.

BIT 408

DIGITAL IMAGE PROCESSING
(ELECTIVE-III)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Image processing: Introduction, Fundamental steps, Components. Elements of visual perception, image sampling and quantization, some basic relationships between pixels.

Intensity Transformations Some Basic Intensity Transformation Functions, Histogram Processing

UNIT- II

Spatial Filtering: Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters

Filtering in the Frequency Domain: Preliminary Concepts, Image Smoothing using Frequency Domain Filters, Image Sharpening Using Frequency Domain Filters.

UNIT- III

Image Restoration and Reconstruction : A Model of the Image degradation/Restoration Process, Noise Models, Restoration in the Presence of Noise Only—Spatial Filtering, Minimum Mean Square Error (Wiener) Filtering

Morphological Image Processing: Preliminaries, Erosion and Dilation, Opening and Closing

UNIT- IV

Image Segmentation: Fundamentals, Point, Line, and Edge Detection, Segmentation by Thresholding, Region-Based Segmentation, Segmentation Using Watershed Algorithm.

Representation and Description: Representation, Some Simple Descriptors, Shape Numbers, Fourier Descriptors.

Object Recognition: Patterns and Pattern Classes, Matching: Minimum distance classifier, correlation.

UNIT-V

Color Image Processing: Color Fundamentals, Color Models, Pseudo color Image Processing.

Image Compression: Fundamentals, Compression Techniques, Lossless Compression, Lossy Compression, Measuring Information, Lossless Compression, Huffman Encoding, Arithmetic Coding, LZW, Run Length, Predictive Coding

Suggested Reading:

1) Rafael C Gonzalez and Richard E Woods, "Digital Image Processing", Pearson Education, 3rd Edition.
2) Vipula Singh, "Digital Image Processing with MatLab and lab View" Elsevier
3) Milan Sonka, Vaclav Halvac and Roger Boyle, "Image Processing, Analysis, and Machine Vision", Second Edition, Thomson Learning Publishers.
4) Kenneth R.Castleman, "Digital Image Processing", Pearson Education.
5) Rapel C Gonzalez , Richard E Woods and Steven L Eddins, "Digital Image Processing using MATLAB", Pearson Education.

BIT 409

GRID COMPUTING
(ELECTIVE-III)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Introduction to Grid Computing: Grid Computing Concept, History of Distributed Computing

Computational Grid Applications, Grid Computing Infrastructure Development, Grid Computing

Software Interface Job Submission: Introduction, Globus Job Submission, Transferring Files.

UNIT-II

Schedulers: Scheduler Features, Scheduler Examples, Grid Computing Meta-Schedulers,

Distributed Resource Management Application (DRMAA).

Security Concepts: Introduction, Symmetric Key Cryptography, Asymmetric Key Cryptography, (Public Key Cryptography), Public Key Infrastructure, Systems/Protocols Using Security Mechanisms.

Grid Security: Introduction, Grid Security Infrastructure (GSI), Delegation, Higher-Level Authorization Tools.

UNIT-III

System Infrastructure I: Web Services: Service-Oriented Architecture, Web Services and Web Service Implementation.

System Infrastructure II: Grid Computing Services: Grid Computing and Standardization Bodies, Interacting Grid Computing Components, Open Grid Services Architecture (OGSA), WSRF.

User-Friendly Interfaces: Introduction Grid Computing Workflow Editors, Grid Portals.

UNIT-IV

Grid-Enabling Applications: Introduction, Parameter Sweep, Using an Existing Program on Multiple Grid Computers, Writing an Application Specifically for a Grid, Using Multiple Grid Computers to Solve a Single Problem.

UNIT-V

Case Studies:

Globus: Overview of Globus Toolkit 4, Installation of Globus, GT4 Configuration, Main Components and programming Model, Using Globus.

gLite: Introduction, Internal Workings of gLite, Logging and Bookkeeping (LB), Security Mechanism Using gLite.

Resource management using Gridway and Gridbus.

Scheduling using Condor, SGE, PBS, LSF Grid scheduling with QoS.

Suggested Reading:

1) Barry Wilkinson, "Grid Computing Techniques and Applications", CRC Press, 2010.
2) Frederic Magoules, Jie Pan, Kiat-An Tan, Abhinit Kumar, "Introduction to Grid Computing" CRC Press, 2009.
3) Vladimir Silva, "Grid Computing for Developers ", Dreamtech Press, 2006.
4) Ian Foster, Carl Kesselman. "The Grid 2- Blueprint for a new computing Infrastructure", Elsevier Series, 2004.
5) Fran Berman, Geoffrey Fox. Anthony J.G Hey, "Grid Computing: Making the Global Infrastructure a Reality", Wiley, 2003.
6) Joshey Joseph, Craig Fellenstein, "Grid computing", IBM Press, 2004.

BIT 410

CPLD AND FPGA ARCHITECTURE (ELECTIVE-III)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Review of Logic Design, Implementation with NAND – NOR gates, designing with multiplexers, implementation of logic functions with look-up tables, minimization of combinational functions based on a) Circuit size, gates and literals i.e. space & power b) number of levels of logic i.e. time or circuit depth.

The Quine-McCluskey Algorithm, Multi level logic minimization, covering, factored forms, technology mapping, review of finite state machines, one hot encoding

UNIT-II

Programmable Logic: Introduction, programmable logic devices (PLDs), SPLDs, CPLDs, fundamentals of PLD circuits, PLD symbology, PLD architectures: Progrmmable Read Only Memories (PROMs), Programmable Array Logic (PAL), ALTERA CPLDs

UNIT-III

FPGAs: Introduction, Programming Technologies: SRAM, Antifuse, EPROM and EEPROM Xilinx FPGAs, Actel, Altera, Concurrent Logic FPGAs. Crosspoint Solutions FPGA, translation to XNF format, Partition, Place and route, Technology mapping for FPGAs: Logic Synthesis, logic Optimization, Lookup Table Technology Mapping, Mapping into Xilinx 3000 CLBs, Multiplexer Technology, Mapping.

UNIT-IV

Logic Block Architecture: Logic Block functionality Versus area-efficiency, Impact of Logic Block Functionality in FPGA performance, Routing for FPGAs: Segmented Channel Routing, Routing for Symmetrical FPGAs, CGE detailed router Algorithm. Flexibility of FPGA routing architectures: Logic Block, Connection Block, Trade offs in Flexibilities of the S and C blocks, A theoretical model for FPGA routing.

UNIT – V

Platform FPGA architectures, Multi-FPGA Systems: Xilinx Virtex II Pro Platform FPGA, Altera Stratix Platform FPGA, Serial I/O, Memories, CPUs and Embedded Multipliers, Multi FPGA systems: Interconnecting Multiple FPGAs, partitioning, Novel architectures.

Suggested Reading:

1. Park K. Chan / Samiha Mourad, "Digital Design using Field Programmable Gate Arrays", Pearson, 1994 (Unit-I)
2. Ronald J Tocci, Neal S. Widmer, Gregory L. Moss, "Digital Systems: Principles & Applications", 10th Edition, Pearson, 2009 (Unit-II)
3. Stephen Brown Zvonko Vranesic – Fundamentals of Digital Logic with VHDL design, McGraw Hill – 2000 (Unit I & II).
4. Stephen D. Brown, Robert J Francis, Jonathan Rose, Ivonko G. Vranesic, "Field Programmable Gate Arrays", Springer International Edition, First Indian Print 2007(Unit III & IV)
5. Wayne Wolf, "FPGA-based System Design", Pearson Education, First Impression, 2009 (Unit V)
6. Stephen M. Trimberger, "Field Programmable Gate Array Technology" Springer International Edition", First Indian Reprint 2007.
7. Michel John Sebastian Smith "Application – Specific Integrated Circuits", Pearson Education, First Indian reprint 2000.

BIT411

SOFTWARE REUSE TECHNIQUES (ELECTIVE-III)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Software reuse success factors, Reuse driven software engineering as business, Object oriented software engineering, Applications and Component subsystems, Use case components, Object components.

UNIT-II

Design Patterns — Introduction. Creational Patterns — Factory Pattern, Factory Method, Abstract Factory Pattern, Singleton Pattern, Builder Pattern, Prototype Pattern.

UNIT-III

Structural Patterns — Adapter Pattern, Bridge Pattern, Composite Pattern, Decorator Pattern, Façade Pattern, Flyweight Pattern, Proxy Pattern. Behavioral Patterns — Chain of responsibility Pattern, Command Pattern, Interpreter Pattern.

UNIT-IV

Behavioral Patterns—Iterator Pattern, Mediator Pattern, Memento Pattern, Observer Pattern, State Pattern, Strategy Pattern, Template Pattern, Visitor Pattern. Architectural Patterns—Layers, Pipes and Filters, Black board.

UNIT-V

Object Oriented Business Engineering –Business Process Reengineering, Software Engineering Process in reuse business. Component System Engineering – building flexible components systems, requirement analysis, robustness analysis, design, implementation and testing the component system.

Suggested Reading:

1) Ivar Jacabson, Martin Griss, Patrick Johnsson,"Software Reuse: Architecture, Process and Organization for Business Success". Pearson Education,2003.
2) James W Cooper, "Java Design Patterns, a tutorial", Pearson Education, 2003.
3) Frank Buschmann, et al., "Pattern Oriented Software Architecture – Volume I" John Wiley & Sons,1996.

BIT412

SEMANTIC WEB (ELECTIVE-III)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

The Future of the Internet: Introduction, Syntactic Web, Semantic Web, Working of Semantic Web, What is not a Semantic Web, Side Effects.
Ontology: Definitions, Taxonomies, Thesauri and Ontologies, Classifying Ontologies, Web Ontology Description language, Ontologies-Categories-Intelligence .

UNIT-II

Knowledge Description in Description Logic: Introduction, Example, Family of Attributive Languages, Inference problems.
RDF and RDF Schema: Introduction, XML Essentials, RDF, RDF Schema.

UNIT-III

OWL: Introduction, Requirements for Web Ontology Description Languages, Header Information, Versioning and Annotation Properties, Properties, Classes, Individuals, Data types

Rule Languages: Introduction, Usage Scenarios, Datalog, RuleML, SWRL, TRIPLE.

UNIT-V

Semantic Web Services: Introduction, Web Service Essentials, OWL-S Service Ontology, OWL-S Example.

Methods for Ontology Development: Introduction, Uschold and King Ontology Development Method, Toronto Virtual Enterprise Method, Methontology, KACTUS Project Ontology Development Method, Lexicon-Based Ontology Development Method, Simplified Methods.

UNIT-V

Ontology Sources: Introduction, Metadata, Upper Ontologies.
Software Agents: Introduction, Agent Forms, Agent Architecture, Agents in the Semantic Web Context.

Applications: Introduction, Horizontal Information Products, Open academia, Bibster, Data Integration, Skill Finding, Think Tank Portal, e-learning, Web Services.

Suggested Reading:

1) Karin K Brietman, Marco Antonio Casanova, Walter Truszkowski, "Semantic Web – Concepts", Technologies and Applications. Springer 2007.
2) Grigoris Antoniou, Frank van Harmelen, "A Semantic Web Primer", PHI 2008.
3) Liyang Yu, "Semantic Web and Semantic Web Services", CRC 2007.

BIT431

VLSI DESIGN LAB

Instruction	3	Periods per week
Duration of University Examination	3	Hours
University Examination	50	Marks
Sessional	25	Marks

1. Switch level modeling using Verilog
   a) Logic gates b) AOI and OAI gates
   c) Transmission gate d) Complex logic gates using CMOS
2. Structural Gate-level Modeling [With and Without delays] – Digital circuits using gate primitives – using Verilog.
   a) AOI gate b) Half adder and full adders
   c) MVX using buffers d) S-R latch etc.
3. Mixed gate –level and Switch-level modeling using Verilog-usage of primitives, modules and instancing and understanding the hierarchical design.
   a) Constructing a 4-input AND gate using CMOS 2-input NAND and NOR gates.
   b) Constructing a decoder using CMOS 2-input AND gates and NOT gates etc.
4. RTL Modeling of general VLSI system components.
   a) MUXes b) Decoders
   c) Priority encodes d) Flip-flops e) Registers.
5. Synthesis of Digital Circuits
   a) Ripple carry adder and carry look-ahead adder
   b) array multiplier
6. Verilog code for finite state machine
7. Modeling of MOSFET
8. Stick diagram representations. Simple layouts of Inverter. Understanding the concepts of Design Rule checking.
9. Fault Modeling for Stuck-at-O and Stuck-at-1 faults.
10. Clock generation circuit(study)

BIT 432

MIDDLEWARE TECHNOLOGIES LAB

Instruction	3	Periods per week
Duration of University Examination	3	Hours
University Examination	50	Marks
Sessional	25	Marks

1. Create a distributed name server (like DNS) RMI
2. Create a Java Bean to draw various graphical shapes and display it using or without using BDK
3. Develop an Enterprise Java Bean for student Information System.
4. Develop an Enterprise Java Bean for Library operations.
5. Create an Active-X control for Timetable.
6. Develop a component for converting the currency values using COM / .NET
7. Develop a component for browsing CD catalogue using COM / .NET
8. Develop a component for retrieving information from message box using DCOM/.NET
9. Develop a middleware component for retrieving Stock Market Exchange information using CORBA
10. Develop a middleware component for retrieving Bank Balance using CORBA.

BIT433

PROJECT SEMINAR

Instruction	3	Periods per week
Sessional	25	Marks

The objective of the project seminar is to actively involve the student in the initial work required to undertake the final year project. It may comprise of:

- Problem definition and specifications.
- A broad understanding of the available technologies/ tools to solve a problem of interest.
- Presentation (Oral and Written) of the project.

Seminar topics may be chosen by the students with advice from the faculty members.

First 4 weeks of IV year 1st semester will be spent on special lectures by faculty members, research scholar speakers from industries and R&D institutions. The objective of these talks is to be expose students to real life / practical problems and methodologies to solve them.

A seminar schedule will be prepared by the coordinator for all the students. It should be from the 5th week to the last week of the semester and should be strictly adhered to.

Each student will be required to

1. Submit a one page synopsis of the seminar to be delivered for display on notice board.
2. Give a 20 minutes presentation followed by 10 minutes discussion.
3. Submit a technical write up on the talk delivered.

At least two teachers will be associated with the evaluation of the project seminar for the award of the sessional marks which should be on the basis of performance on all the three items stated above.

In the first Semester the student is expected to complete problem definition, requirements specification and analysis, design.