Kaleem Fatima
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Scopus:
https://www.scopus.com/authid/detail.uri?authorId=26430845600

Education:

Ph.D: Hardware Routing Accelerators for VLSI Design; Osmania University, 2009.
MTech: Digital Electronics and Communication Systems, MCE Hassan, Mysore University, 1991.

Work Experience:

- 31 years teaching
- Industry exposure: MTech Internship cum project, "Radar Signal Processor using ADSP-2100 microprocessor" at LRDE, Bangalore, 1990-91 for a period of 9 months

Selected subjects taught:

- Microprocessors and Microcontrollers
- Digital Electronics/Adv. Digital Design
- Digital Communications
- Digital design using Verilog HDL
- VLSI Design
- Electronic Devices and Circuits

Research areas of interest:

- Digital Vedic Arithmetic Circuits
- Multipliers
- IOT security and applications
- Embedded Systems design
- Robotic Manipulators

PhDs Guided: 4 **PG Guided:** 10+

PhDs under progress: 6

Undergraduate projects: 30+

Employment History: @ MJCET:

- 2009 – Till date: Professor
- 2010 – 2017 : Professor and Head (ECE)
- 1999 – 2009 : Associate Professor
- 2003 – 2005 : Head (ECE)
- 1993 – 1999 : Assistant Professor

Professional Memberships:

- IEEE Member : 2001 – 2010
- IEEE Senior Member : 2010 – till date
- Member IEEE Circuits and Systems Society [2012 – till date]
- Member Women In Engineering (WIE), [2012 – 2017]
- Fellow IETE, [2008 – life membership]
- Member ISTE [1996 – life membership]

Responsibilities:

- HOD, Electronics and Communication Engineering [2003 -05] & [2010-2017]
- Supervisor for PhD, OU, [2012 onwards]
- Member, BOS, OU, [2003 -05] & [2010-2017]
- Member DRC, OU, [Aug 2014- Aug 2016]
- Member, NBA Core Committee, MJCET [2013 – 2019]
- Member, IQAC, MJCET, [2014-2023]
- Leading role in establishment of Research Center at ECED, MJCET, year 2012-13
- Incharge, Student Course Counceling/General Counseling, including formation of guidelines, MJCET [2015 – 2017]
- Chair, Department Advisory Committee, ECED [2013 – 2017]
- Member Program Assessment Committee, ECED [2017 – till date]
- Member R & D Committee, MJCET, [2013 – 2018]
- Project Coordinator, ECE Dept. [2010 – till date]

Professional Contributions:

- Founder member, IEEE CAS/EDS Joint Chapter at IEEE Hyderabad Section, year 2012
- Chair, IEEE CAS/EDS Joint Chapter, Hyd. Section [2016-2018]

- Vice Chair, IEEE CAS/EDS Joint Chapter, Hyd. Section [2014-2016]
- Secretary, IEEE CAS/EDS Joint Chapter, Hyd. Section [2012-2014]
- Vice Chair, IEEE Women In Engineering, WIE, Hyd. Section [2012]
- IEEE Branch Counselor, MJCET, [2011 – 2017]
- IEEE Branch Mentor, MJCET, [2002 – 2011]
- Chapter Advisor, IEEE CAS chapter, MJCET, [2017 – till date]
- Started 4 MJCET IEEE chapters – CS, WIE, PES, CIS, CAS duration [2011 – 2013]

Contributions in Conferences:

- **Organizing Co-chair:** IEEE Asia-Pacific Conference on Postgraduate Research on Microelectronics and Electronics; ***PrimeAsia 2012***, BITS-Pilani, Hyderabad Campus, December 5-7, 2012
- **Publication Co-Chair:** IEEE Asia-Pacific Conference on Postgraduate Research on Microelectronics and Electronics; ***PrimeAsia 2013***, Gitam University Vishakapatnam Campus, December 19-21, 2013
- **Publication Co-Chair:** IEEE Asia-Pacific Conference on Postgraduate Research on Microelectronics and Electronics; ***PrimeAsia 2015***, VCE, OU, Hyderabad, November 27-29 2015
- **Tutorial Co-Chair:** MOS – AK India 2019 Conference, Joint Chapter CAS/EDS, in collaboration with Modeling of Systems Working Group (MOS-AK), Switzerland and IIT Hyderabad, 25th – 27th February 2019
- **Conference Chair:** National Conference on Circuits, Signals and Systems (NCCSS – 2015); organized by Dept. of ECE, MJCET, 22nd – 24th January, 2015
- **IEEE CAS Liaison:** VLSID 2017, 30th International Conference on VLSI Design; 16th International Conference on Embedded Systems, 7th -11th January 2017
- **Session Chair:** at various conferences: VLSID 2012, PrimeAsia 2012, PrimeAsia 2013, PrimeAsia 2015, MOS- AK 2019, IEEE – HYDCON 2020, ICETE 2023(OU)
- **Technical Review Committee** member for prestigious conferences

NPTEL Online Certification:

- Awarded Elite+Gold (Topper – 1%) score 99%, "Microprocessors and Interfacing" Jan-Apr 2020 (12 week)
- Awarded Elite+Gold (Topper – 1%) score 95%, "Switching Circuits and Logic Design" Jul-Oct 2019 (12 week)

Patent: 1 -- Govt. of India

- Grant of Utility Patent titled " A Pneumatic Quadruped Robot and a method of Preventing Accidents thereof" (Patent No. 384439 dated 31-12-2019) for a term of 20 years

Awards and Recognitions:

- **"IEEE R10 Outstanding Branch Counselor Award"** for the year 2011 (Asia Pacific region)
- **Felicitated by Chairman,** SUES & Board Members on 18-12-2012
- **Felicitated by Alumni ECE,** August 24th , 2024 at Texas, Austin, USA (1984, 1992, 1995, 1996, 1998, 2004, 2011, 2014, 2016, 2022, 2024 pass out batch students were present during felicitation)
- **"Faculty Excellence Award"** for the year 2007-2008 by Principal MJCET.
- **Received appreciation and incentive** award for utility patent grant no: 384439 from Hon. Secretary, SUES.
- **Received appreciation** and cash award in July 2006 for obtaining Xilinx ISE/EDK tools and XUPV2P Development Board under Xilinx University donation program. Principal MJCET

Google Scholar
http://scholar.google.co.in/citations?user=s3Nt420AAAAJ

Journal Publications (Scopus): 16 **SCI/SCIE** : 5
Conference proceedings (Scopus indexed): 18
Citations: 66
H Index: 4 I-10 Index: 1

PhD Awarded Students:

Dr. Salma Fauzia:

1. Area of Research: "Qos Based Directional Routing In Free Space Optical Mobile Ad-Hoc Networks", Ph.D Awarded September 2020

Dr. Ganti Srilakshmi:

2. Area of Research: Model for Vinculum arithmetic – case study on floating point multiplier", Ph.D Awarded January 2023

Dr. Shefali Madikanti

3. Area of Research: "Performance Analysis of Carbon Nanotube Interconnects in Ultra Deep Submicron ULSI Circuits", Ph.D. Awarded May 2023

Dr. Prathibha

4. Area of Research: "A Lightweight Security Framework for IOT Smart Devices", Ph.D Awarded August 2023

Current PhD students:

Ms. Maliha Naaz

5. Area of Research: "A QFN Bondwire Inductance Based Self-Startup Ultra Low Voltage Boost Converter for Thermal Energy Harvesting". Submitted thesis

Mr. Mohammed Osman

6. Area of Research: "Compound Metric Based Trust Routing in IOT Networks Using Bio-Inspired Optimization", Submitted thesis

Mr. Chintam Shravan

7. Area of Research: Performance Optimisation of Gc-eDRAM Memory Controller in Multi-Processor SoC", Submitted thesis

Ms. Divyabeebi Reddy

8. Area of Research: "Analysis and Optimization of Dual Material Junctionless TreeFET for Ultra-low power applications" completed Pre-submission seminar

Selected UG/PG Projects guided (SUES funded and/or published):

1. MARTIN: ROS Based Autonomous Mobile Manipulator Robot (paper published in Proceedings of ICETE Conference" (2023)
2. SARM: ROS Based Synergetic Articulated Robotic Manipulator (Autonomous Bot) (2022)
3. Design And Fabrication of Pneumatic Quadruped Robot (2018) (patent granted 2021)
4. RAES: Rehabilitation Assistance Exo-Skeleton (2020)
5. Quadcopter for navigation, imaging and surveillance (2017)
6. Quadcopter: Semi Controlled Aerial Vehicle (2015)
7. Implementation Of Two Chooses One Physical Unclonable Function for IOT Security (2020)
8. IBM Watson - Personal Health Assistant (2018)
9. A Novel Architecture for the Computation of 2D-DWT and its Implementation on Virtex-II Pro FPGA (2007 paper published in Proc. of International Conference on Computational Intelligence and Security, Harbin Institute of Technology, Harbin, China, pp: 531 - 535 Dec, 15 -19, 2007**. ISBN: 0-7695-3072-9**

List of Publications:

I. International Journal:

1. Beebireddy Divya, Kaleem Fatima, and L. Nirmala Devi, "Optimizing Device Dimensions for Dual Material Junctionless Tree-FET: A Path to Improved Analog/RF Performance", ECS Journal of Solid State Science and Technology, Vol 13, No, 7, 073003, 2024, doi:10.1149/2162-8777/ad5c9e. (SCIE - Published).
2. Beebireddy Divya, Kaleem Fatima, and L. Nirmala Devi, "Impact of Interface Trap Charges on the Electrical and Analog/RF Performance of Dual Material Junctionless Tree FETs", Scope.
3. Beebireddy Divya, Kaleem Fatima, and L. Nirmala Devi, "Enhancing DM Junctionless Tree-FET Performance Through Spacer Optimization: A Comprehensive DC and RF Analysis", Journal of Electronic Materials. (SCIE - Under Review).
4. Unnisa, N., Tatineni, M., Fatima, K., Pasha, M.M. "Intelligent deep learning-aided future beam and proactive handoff prediction model in Unmanned Aerial Vehicle-assisted anti-jamming Terahertz communication system"; *International Journal of Communication Systems*, 2023, 36(13), e5504; (SCI)
5. Maliha Naaz, Kaleem Fatima, B. Rajendra Naik, "A Transient Enhanced Capacitor-less Low dropout Regulator Using 180nm CMOS technology". *International Journal on Recent and Innovation Trends in Computing and Communication*, 11(9), 4089–4094. https://doi.org/10.17762/ijritcc.v11i9.9769
6. M Naaz, MA Sohel, K Fatima, MA Raheem, "Design of low power notch filter for biomedical applications"; *International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering*, IJIREEICE 4 (12), 75-79
7. Osman, M., Fatima, K., Kumar, P.N., "Compound Metric Assisted Trust Aware Routing for Internet of Things through Firefly Algorithm"; *International Journal of Intelligent Engineering and Systems*, 2023, 16(3), pp. 280–291; *Open access;* https://doi.org/10.17762/ijritcc.v11i10.8713.
8. Osman, M. Fatima, K., & Kumar, P. N. (2023) "Communication and Content Trust Aware Routing for Clustered IoT Network". *International Journal on Recent and Innovation Trends in Computing and Communication*, 11(10),16141623.
9. Shravan, C., Fatima, K. & Sekhar, P.C. "Design and Development of Novel Refresh Technique for Gain Cell Embedded DRAM". SN Computer Science, 2023, 4(6) 786 . https://doi.org/10.1007/s42979-023-02223-z
10. Shravan, C., Fatima, K., Paidimarry, C.S. "Design and Develop Low-Power Memory Controller for Gain Cell–Embedded Dynamic Random-Access Memory Cell Using Intelligent Clock Gating" *Telecommunications and Radio Engineering*, 2024, 83(8), pp. 83–94; ISSN Print:0040-2508 ISSN Online:1943-6009
11. Shravan, C., Fatima, K., Sekhar, P.C. "Design and Develop Efficient Arbitration Technique to Handle the Multiple Refresh Requests in Multi-Processor SoC"; *International Journal on Recent and Innovation Trends in Computing and Communication*, 2023, 11, pp. 341–350 https://doi.org/10.17762/ijritcc.v11i8s.7214 (open access)
12. M. Shefali, Kaleem Fatima, P. Uma Sathyakam "Frequency Response Analysis of CNT bundle Interconnects," *International Journal of Electronics*, 2023, 11(4), pp. 439–448 https://doi.org/10.1080/21681724.2022.2117849
13. M. Shefali, Kaleem Fatima, P. Uma Sathyakam "Performance Analysis of CNT bundle interconnects in various low-k dielectric media," *ECS Journal of Solid-State Science and Technology*, 2022, 11(6), 061003

14. M. Shefali, Kaleem Fatima "ULSI Interconnects Scaling: Trends, Challenges and their Solutions," *International Journal of Recent Advances in Multidisciplinary Topics*,Volume 3, Issue 3, March 2022, p132-133, 2582-7839
15. Prathibha, L., and Kaleem Fatima. "A Novel High-Speed Data Encryption Scheme for Internet of Medical Things Using Modified Elliptic Curve Diffie–Hellman and Advance Encryption Standard." *International Journal of Image and Graphics* (2022): 2340004.
16. Fauzia S., Fatima K. "Performance Evaluation of AODV Routing Protocol for Free Space Optical Mobile Ad-Hoc Networks". *Intelligent Systems Technologies and Applications.* ISTA 2017, vol 683. , 74-83, Springer, Cham.
17. Fauzia, S., Fatima, K," QoS based Routing for Free Space Optical Mobile Ad Hoc Networks.,"2019 *International Journal of Vehicle Information and Communication Systems* (IJVICS).
18. Fauzia, S., Fatima, K," Routing in Optical Mesh Networks - A QoS Perspective.," 2018 International Journal of Ad hoc, Sensor & Ubiquitous Computing (IJASUC).
19. Nazeerunnisa and Dr.Kaleem Fatima,"ANFIS Based Performance Analysis In Uplink OFDMA Rician Fading Channel", International system of VLSI system design and communication system. ISSN 2322-0929 Vol.03, Issue.07, September-2015.
20. G Sreelakshmi, K Fatima, BK Madhavi, "A Frame Work for Decimal Floating Point Multiplier Using Vinculum Multipliers", *Journal of New Insights into Physical Science, 152, 2021*
21. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "Efficient Realization of Vinculum Vedic BCD Multipliers for High Speed Applications", Journal of Circuits and Systems, 2018, vol 9, with ISSN 2153-1293 , DOI:10.4236/cs.2018.96009 June 2018.
22. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "Hybrid Signed Digit Parallel and Multi Operand BCD Adders" *International Journal of Pure and Applied Mathematics,* Volume 20, No.6 1337-1391 with ISSN number1314-1395, 2018.
23. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "Area-Delay-Power Efficient Booth Encoded Reversible Multiplier using Compressors" *Journal of Innovation in Electronics and Communication Engineering,* Jul-Dec 2015 Volume5, Issue2 ISSN: 2249-9946.
24. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "High Performance BCD Adder-Subtractor Using Reversible Logic" *International Journal of Engineering Inventions,* Nov-Dec 2012 ISSN: 2278-7461.
25. Kaleem Fatima and Rameshwar Rao, "FPGA Solution for Multi-layer Maze Routing*" IETECH International Engineering and Technology Journal of Communication Techniques,* Vol: 2, No: 2, pp 78-83, 2008. (ISSN 0973 8053)
26. Kaleem Fatima and Rameshwar Rao, "A Hardware Router for Multi-Terminal Nets" *IETECH International Engineering and Technology Journal of Information Systems*. (ISSN 0973 8096)
27. K Fatima, R Rao, "Design of a hardware accelerator for multi-layer maze routing in VLSI and its implementation on Virtex-II pro" *IET Digital Library, 817-821, 2007*
28. S Hussain, Z Hussain, K Fatima, "A VLSI Implementation of FSM-based programmable Memory Built-In Self Test (MBIST) Controller"
29. Kaleem Fatima, S. Vijay Gopal and N. Zeeshan Nadeem, "A Novel Architecture for the Computation of 2D-DWT and its Implementation on Virtex-II Pro FPGA (2007 paper published in Proc. of International Conference on Computational Intelligence and Security, Harbin Institute of Technology, Harbin, China, pp: 531 - 535 Dec, 15 -19, 2007**. ISBN: 0-7695-3072-9**

II. Conference Proceedings:

1. Naaz, M., Fatima, K., Naik, B.R., ... Ahmed, S.S., Ashher, M.S. “Design of DC-DC Boost Converter Using PFM Switching Technique”; *Proceedings of 5th International Conference on 2023 Devices for Integrated Circuit, DevIC 2023*, 2023, pp. 368–371
2. Naaz, M., Fatima, K., Naik, B.R., ... Jabeen, A., Hussain, S.J. “A DC-DC Boost Converter using PWM with 65%efficiency”; *Proceedings of 5th International Conference on 2023 Devices for Integrated Circuit, DevIC 2023*, 2023, pp. 377–382; https://doi.org/10.1109/DevIC57758.2023.10134808
3. Naaz, M., Kaleem Fatima, B. Rajendra Naik, “A Survey Paper on Capacitor-Less Low Dropout Regulator,” *2022 International Conference on Electrical, Computer and Energy Technologies* (ICECET), Prague, Czech Republic, 2022, pp. 1-6, https://doi.org/10.1109/ICECET55527.2022.9872998
4. Prathibha, L., and Kaleem Fatima. "Exploring Security and Authentication Issues in Internet of Things." *2018 Second International Conference on Intelligent Computing and Control Systems* (ICICCS). IEEE, 2018.
5. Beebireddy Divya, Kaleem Fatima, and L. Nirmala Devi, “Reliability Analysis of Dual Material Junctionless Tree FET for High-Performance Applications", *IEEE 21st India Council International Conference* (INDICON), 19th − 21st Dec, 2024, IIT Kharagpur, Kharagpur, India. (IEEE – in Press).
6. Prathibha, L., and Fatima, K., "Exploring Security and Authentication Issues in Internet of Things," *2018 Second International Conference on Intelligent Computing and Control Systems (ICICCS)*, Madurai, India, 2018, pp. 673-678.
7. Fauzia, S., Fatima, K,” A New Approach to Directional Routing in MANETs”, 2019 IEEE International Conference on Innovative Technologies in Engineering IEEE, ICITE, OU, 2018 978-1-5386-5080- 6/18
8. Fauzia, S., and Fatima, K., "Routing in FSO MANETs -- QoS and directionality," *2014 Eleventh International Conference on Wireless and Optical Communications Networks (WOCN)*, Vijayawada, 2014, pp. 1-5. doi: 10.1109/WOCN.2014.6923062
9. G Sreelakshmi, K Fatima, BK Madhavi, “Design and implementation of Vinculum Binary Coded Decimal multipliers using vinculum binary coded decimal compressors”, *2019 International Conference on Communication and Electronics Systems*
10. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi“ Implementation of High Speed Vedic BCD Multiplier using Vinculum Method”; *Proceedings of IEEE Region 10 Conference (TENCON)*, 147-151 22nd to 25th Nov, 2016, 978-1-5090-2597-8/16/
11. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi “Designing of Digital circuits using Vedic mathematics for Engineering Applications” at the 3rd International Vedic Mathematics Conference at RV College of Engineering Bengaluru, 23-25 August 2018.
12. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi “Hybrid Signed Digit Parallel And Multi Operand BCD Adders” International Conference ICIDEST 17th& 18th April 2018, KCG college of Engineering and Technology, Chennnai.
13. M. Shefali, Kaleem Fatima “Crosstalk Analysis in High Speed ULSI Circuits,”Proceedings of the National Conference on Circuits, Signals and Systems (NCCSS-2015), pp. 27-30
14. G.Sree Lakshmi, Mohammad Salman, Dr.Kaleem Fatima, Dr.B.K.Madhavi “Efficient Vedic Signed Digit Decimal Adder” *proceedings of 4th International Conference on Devices, Circuits and Systems* (ICDCS'18)ISBN: 978-1-5386-3476-9/18/$31.00 ©2018 IEEE 16th & 17th Mar 2018, Electronics and Communication Engineering Karunya Institute of Technology and Sciences

15. G Sreelakshmi, K Fatima, BK Madhavi, "A novel approach to the learning of vinculum numbers in two's compliment method for BCD arithmetic operations", 2018 Second International Conference on Computing Methodologies and and Communication (ICCMC 2018) IEEE Conference Record # 42656; IEEE Xplore ISBN:978-1-5386-3452-3978-1-5386-3452-3/18/$31.00 ©2018 IEEE 475
16. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "Compressor Based 8x8 Bit Vedic Multiplier using Reversible Logic" in the 3rd International Conference on Devices, Circuits and Systems (ICDCS'16) held from 3rd to 5th March 2016 at Karunya University, Coimbatore, India.978-1-5090-2309-7/16/$31.00©2016 IEEE
17. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "Implementation of High Speed Vedic BCD Multiplier using Vinculum Method" TENCON IEEE conference 22nd to 25th Nov 2016. 978-1-5090-2597-8/16/$31.00 c 2016 IEEE Publisher: IEEE Digital Xplorer
18. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "Compressor based 8x8 Bit Vedic Multiplier using Reversible Logic" in the 3rd International Conference on Devices, Circuits and Systems (ICDCS'16) held from 3rd to 5th March 2016 at Karunya University, Coimbatore, India. 978-1-5090-2309-7/16/$31.00©2016 IEEE. Publisher: IEEE Digital Xplorer.
19. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "Area_Delay_Power Efficient Booth Encoded Reversible Multiplier using Compressors" 4th International Conference on Innovations in Electronics and Communication Engineering (ICIECE-2015),August 21st -22nd 2015, Hyderabad, India. ISSN 2249-9946 Vol 5 issue 2G.
20. G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "A High Speed Low Power Multiplier-Accumulator Architecture using Higher Radix Modified Booth Algorithm" at 2nd World Conference on Applied Sciences, Engineering & Technology (WCSET 2013)
21. MA Raheem, H Gupta, K Fatima, O Adil, "A high-speed reversible low-power Error Tolerant Adder", 2012 Asia Pacific Conference on Postgraduate Research in Microelectronics …
22. G.Sree Lakshmi, Kaleem Fatima, Dr.B.K.Madhavi, "A Review of Low Power and High Performance Multipliers and their Hardware Implementations" in Proc of International Conference on Advancements in Engineering and Management, ICAEM 2012, RITs College of Engg. 28th – 29th Feb 2012
23. GS Lakshmi, K Fatima, BK Madhavi, "Design and Implementation of Vedic Multiplier using Reversible Logic
24. Md. Sabir Hussain, Md. Zakir Hussain, Dr. Kaleem Fatima, "High Speed FSM-Based Programmable Memory Built-In Self Test (MBIST) Controller", Accepted in International Conference On Electronics and Communication Engineering (ICECE 2012), to be held on April 28th -29th, 2012., Vizag, India.
25. Prof. Mrs. Kaleem Fatima, Shyam Sundar Mikkili, and Sriram Sankar "The Design and Implementation of a Multiplexed Multi-layer Maze Router " International Conference On Electronics and Communication Engineering (ICECE 2012), April 28th -29th, 2012., Vizag, India.
26. M. A. Raheem and Kaleem Fatima:, "A High Speed Reversible Low Power Error Tolerent Adder" in proceedings of PrimeAsia 2012, held in Dec 7-9, 2012, Bits Pilani, Hyderabad campus.
27.

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