DEPARTMENT OF ELECTRICAL ENGINEERING

LABORATORY MANUAL

INTEGRATED CIRCUITS LAB (EE 383)

For

III/IV B.E I /II SEM EIE & EEE

DEPARTMENT OF ELECTRICAL ENGINEERING
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MUFFAKHAM JAH COLLEGE OF ENGINEERING & TECHNOLOGY

INTEGRATED CIRCUITS LAB

Experiment no:1

ACTIVE FILTERS

AIM: 1.To Design and study the active filters of low pass, high pass, band pass, band reject using op-amps.
2. Calculate the practical filter frequencies and plot the frequency response for each Filter

EQUIPMENTS & COMPONENTS:
1.Active Filters kit
2. 30MHz C.R.O.
3. Multimeter
4. Connecting patch chords.
5. Signal generator

THEORY:

FILTER DESIGN OF FIRST ORDER LOW PASS FILTER:

$$\text{Gain of the filter} = \frac{V_O}{Vin}$$

$$A = 1 + \frac{R_F}{R_1} \text{ (Pass band gain)}$$

$$\text{Higher cut – off frequency } (f_h) = \frac{1}{2\pi RC}$$

1. Choose a value of high cut – off frequency f_H.
2. Select the C (which is provided on the trainer).
3. Calculate the R value

$$\mathbf{R} = \frac{1}{2\pi f_H C}$$ **Adjust the pot resistance equal to the R-value**

FILTER DESIGN OF FIRST ORDER LOW PASS FILTER:

$$\text{Gain of the filter} = \frac{V_O}{Vin}$$

$A_F = 1 + \frac{R_F}{R_1}$ (Pass band gain)

Lower cut – off frequency (f_L) $= \frac{1}{2\pi RC}$

FILTER DESIGN OF FIRST ORDER BAND PASS FILTER:

- A BPF has a pass band between two cutoff frequencies f_H, f_L such that $f_H > f_L$
- When the input frequency is less than the designed frequency of f_L,. the gain of the BPF increases to its 3dB level . After reaching the total pass band region, the gain of the filter is constant up to its designed f_H (high cut off frequency) as stated above.
- Once the input frequency reaches to the f_H, the gain of the BPF decreases to its –3dB level. From that point the gain of the filter gradually decreases.
- There is a phase shift between input and output voltages of BPF in its Pass Band region. This filter passes all frequencies equally well i.e. output and input voltages are equal in amplitude for all frequencies, with the phase shift between the two, a function of frequency. This highest frequency up to which the input and output amplitudes remain equal is dependent on the unity gain bandwidth of the Op – Amp. At this frequency, the phase shift between input and output is maximum.

FILTER DESIGN:

Select the cutoff frequencies of BPF f_H, f_L

f_H = Higher cutoff frequency

f_L = Lower cutoff frequency

$f_C = \sqrt{f_L f_H}$

i) <u>For Low Pass Section</u>:

$f_H = \frac{1}{2\pi R' C'}$ Where $R^1 = \frac{1}{2\pi f_h C'}$

ii) For high pass section:

$$f_L = \frac{1}{2\pi RC}$$

$$\text{Where} \quad R = \frac{1}{2\pi f_L C}$$

If the band pass gain is 4 the gain of the high pass as well as low pass section could be set to 2 i.e. input and feedback resistors must be equal in value. The magnitude of voltage gain is given by

$$\frac{V_O}{V_i} = \frac{A_{FT}(f / f_L)}{\{(1+(f/f_L)^2)(1+(f/f_H)^2)\}^{1/2}}$$

Where A_{FT} = Total Pass band gain

f = Signal input frequency (Hz)

f_L = Low cutoff frequency

f_H = High Cutoff frequency

$f_C = \sqrt{f_L f_H}$

DESIGN OF FIRST ORDER BAND REJECT or NOTCH FILTER:

- A BRF has a stop band between the cutoff frequency f_H&f_L such tha $f_H < f_L$.
- When the input frequency is less than the designed frequency of f_H, the gain of the BRF is constant up to f_H. In other words it allows the frequencies equally well that is output and input voltages are equal in amplitude.
- By increasing the input frequency after f_H, the gain gradually decreases to its center frequency f_C . After this increases to its 3db level. After reaching the total pass band region. The gain of the filter is again constant up to its designed f_H (High cutoff frequency) as stated above.

FILTER DESIGN:

Select the cut off frequency of BRF f_H, f_L

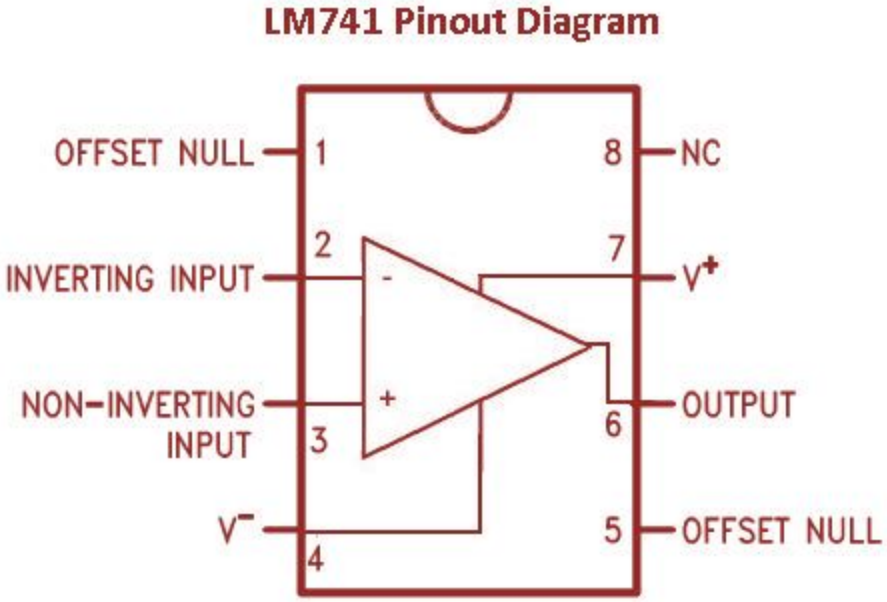
f_H = Higher cutoff frequency
f_L = Lower cutoff frequency

$f_C = \sqrt{f_L f_H}$

$A_f = 1 + \frac{R_F}{R_1}$

If $A_f = 2 \Rightarrow R_F = R_1$

Notch frequency Fn =1 / 2 π RC ,select C calculate R



Circuit Diagram:

Low pass filter:

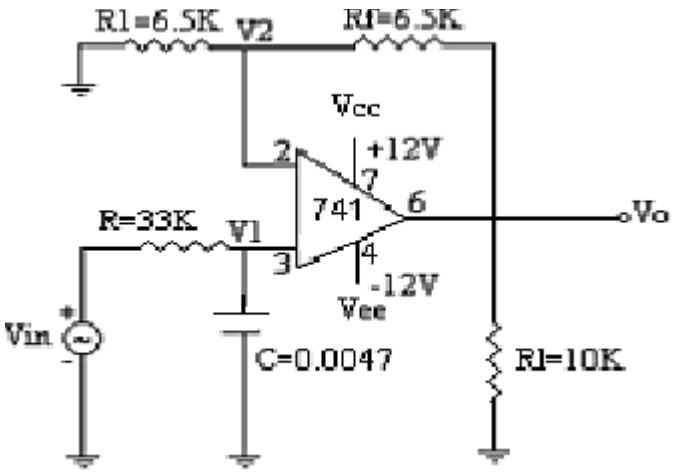


Fig (1) Low pass filter

Lpf → f_h=10 kHz TO 11 kHz

Hpf → f_l=11 kHz

B.P.F → B.W =1 kHz to 4 kHz(1 kHz to 1.75 kHz)

B.R.F → f_h=1.5 kHz →C = 0.1 µf,R= 9.1 K ohms

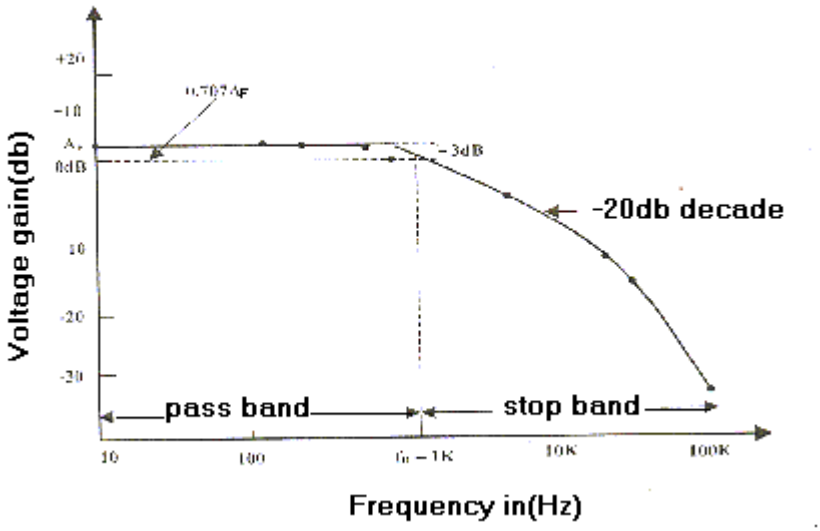


Fig (2) Frequency response

PROCEDURE:

1. Connect the circuit as shown in figure1.using filter kit
2. Choose the R1 and Rf values depending on the pass band gain of the filter Af

   Af=1+(Rf/R1) choose 6.5 K for high Rf and R1 then pass band gain=2
3. Choose a value for high cut off frequency f H
4. Calculate the R using R=1/2ΠfH C where C=0.0047µF.
5. Connect the function generator to the input of the filter of fixed amplitude.of 2 V PP For different values of input signal frequency F. Note the corresponding output voltage.
6. Calculate pass band gain Af which is given by Af=Vo/Vin for different frequencies, note down in the tabular column, record and observe the gain of the filter

7. Plot the frequency response and compare with Fig (2), the frequency response graph of first order Low pass filter

8. Repeat the above procedure for high pass, band pass& band reject filters with their respective design steps and plot their frequency responses

TABULAR COLUMN LPF:

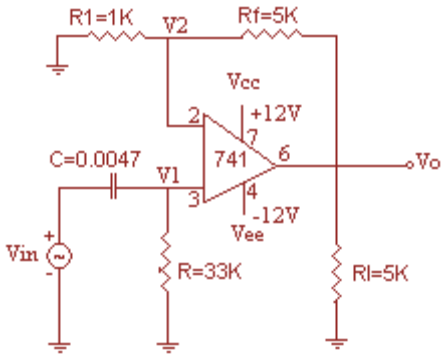
V_{in}=_____

I/P Frequency in Hz	**O/P voltage (V_O) in volts**	**Gain = $\frac{V_O}{V_{IN}}$**	**Gain in dB = 20 log ($\frac{V_O}{V_{IN}}$)**

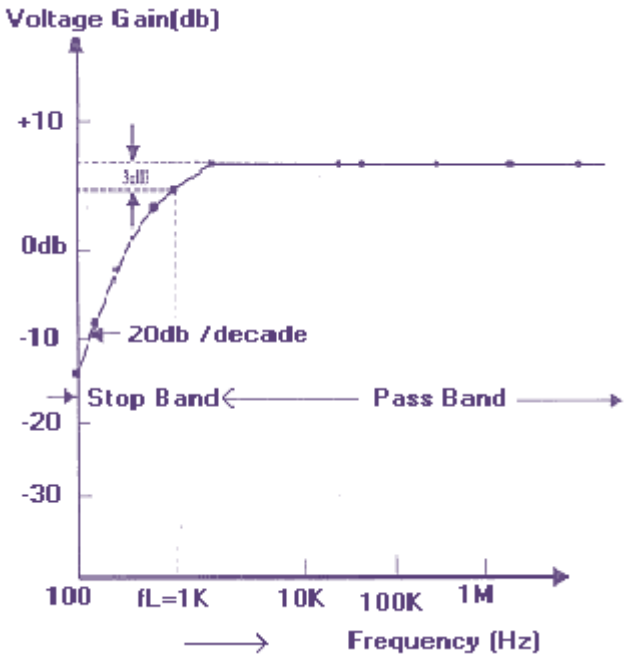
Observe

1. For low frequencies, that is, f<Fh, Vo/Vin=Af
2. When input frequency equals to cut off frequency i.e. f=fH, Vo/Vin=Af/√2=0.707Af
3. For high frequencies i.e. f>fH, Vo/Vin<Af
4. Thus the low pass filter has a constant gain Af upto high cut off frequency. At fH the gain is 0.707Af and after fH it decreases at a constant rate with an increase in frequency.

High pass filter:



(a) High pass filter



(b) Frequency response

TABULAR COLUMN HPF:

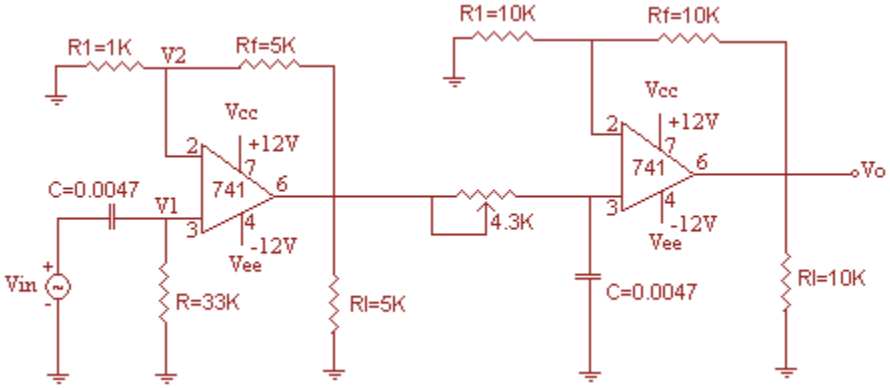
V_{in}=_____

I/P Frequency in Hz	**O/P voltage (V_O) in volts**	**Gain = $\frac{V_O}{V_{IN}}$**	**Gain in dB = 20 log ($\frac{V_O}{V_{IN}}$)**

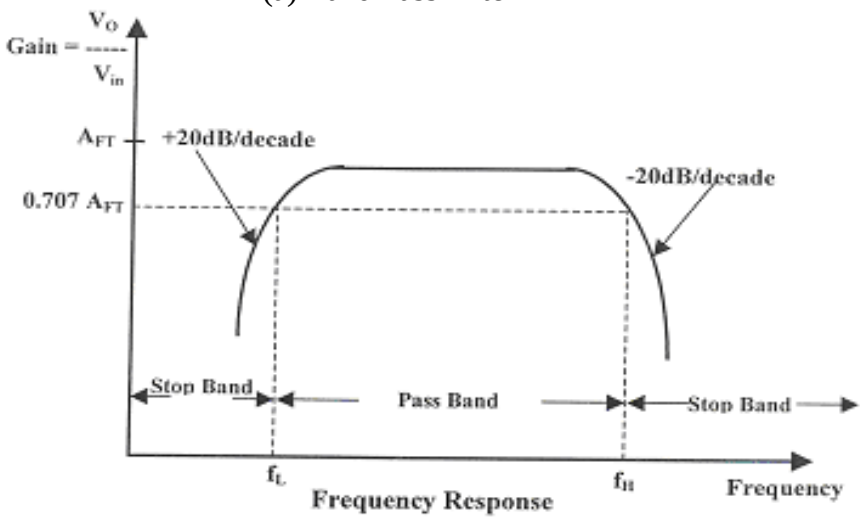
Observe

1. For low frequencies, that is, f<fL, Vo/Vin<Af
2. When input frequency equals to cut off frequency i.e. f=fL
   Vo/Vin=Af/√2=0.707Af
3. For high frequencies i.e. f>fL, Vo/Vin=Af
4. Thus the high pass filter has a constant gain Af from low cut off frequency to Higher cut off frequencies. At fL the gain is 0.707Af below fL it decreases at a Constant rate with an decrease in frequency.

Band Pass Filter:



(a) Band Pass Filter



(b) Frequency response

TABULAR COLUMN BPF:

V_{in}=_____

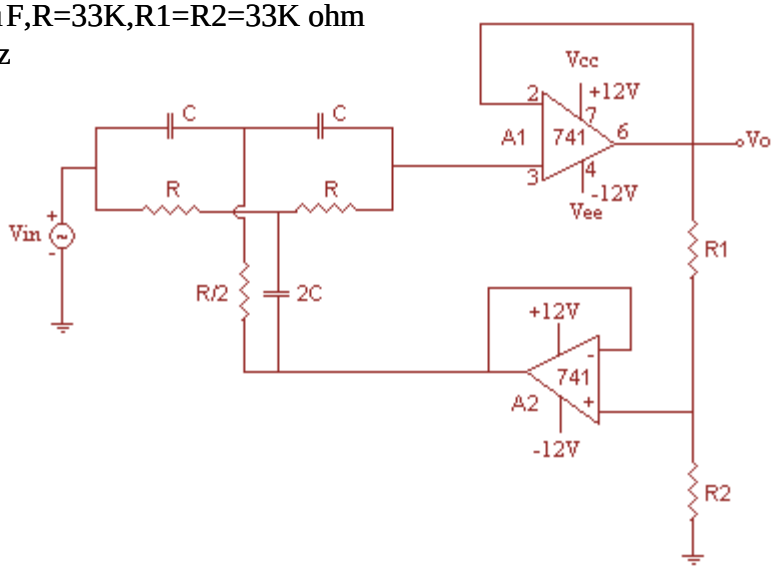
I/P Frequency in Hz	**O/P voltage (V_O) in volts**	**Gain = $\frac{V_O}{V_{IN}}$**	**Gain in dB = 20 log ($\frac{V_O}{V_{IN}}$)**

Observe

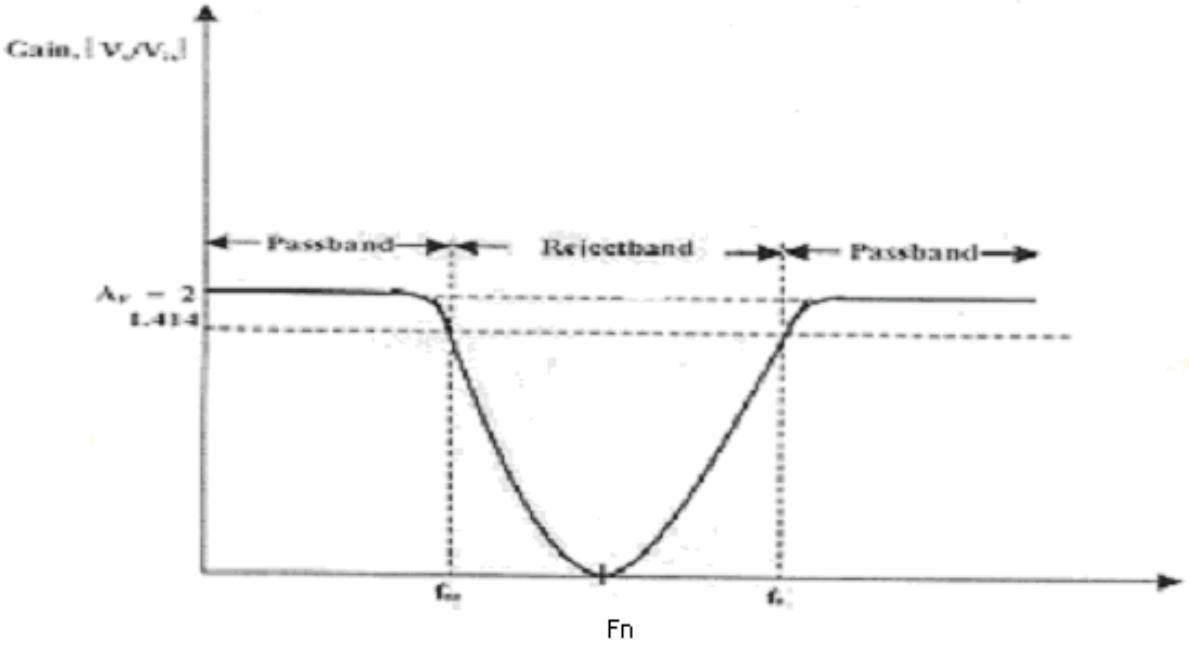
1. For frequencies lower than fL and higher than fH ,Vo/Vin < Af
2. When input frequency equals to cut off frequency i.e. f = fH = fL
   Vo/Vin = Af/√2 = 0.707Af
3. For frequencies ranging from fL to fH, Vo/Vin = Af

Band Reject Filter:

$f_N=1/2\pi RC$
C=0.007µF,R=33K,R1=R2=33K ohm
f_N=4.8kHz



(a) Band Reject Filter



(b) Frequency response

TABULAR COLUMN BRF:

V_{in}=_____

I/P Frequency in Hz	**O/P voltage (V_O) in volts**	**Gain =** $\frac{V_O}{V_{IN}}$	**Gain in dB =** **20 log (** $\frac{V_O}{V_{IN}}$ **)**

Observe

1. For frequencies lower than fL and higher than fH ,Vo/Vin < Af
2.When input frequency equals to cut off frequency i.e. f = fH = fL
Vo/Vin = Af/√2 = 0.707Af
3. For frequencies ranging from fL to fH,Vo/Vin = Af
4.When input frequency equals to cut off frequency i.e. f = fo
Vo/Vin<Af And frequencies other than fo, Vo/Vin = Af

DISCUSSION OF RESULT:

1. Students will observe the frequency responses of various filters and discuss the applications related and will be able to comment on filter specifications.
2. Various regional bands of filters can be observed and selected for specific filters

PRELAB QUESTIONS:

1. What are the applications of filters?
2. What is difference between Active and Passive filters?
3. What are the advantages & disadvantages of Active filters?
4. What happens to filter response as the order of filter increases?
5. Where is all pass filter applicable?
6. What is transition band of a filter?
7. Define Q factor of a filter. how is it related to Corner frequency Fc?

Experiment no:2

ASTABLE MULTIVIBRATOR

AIM: 1.To study and design IC 555 timer as an Astable multivibrator.
2. Calculate the frequency of oscillations & time period of output Waveform.

EQUIPMENTS :
1.IC Trainer kit./ Bread Board
2.20MHz C.R.O.
3.Multimeter
4.Connecting patch chords.
5.variable R.P.S

COMPONENTS:
1. IC 555 Timer
2. Resistors 10 K , 4.7K
3. Capacitors 0.1μF(104), 0.01μF(103)
4. Single stand wires

INTRODUCTION:

The 555 Timer is used in number of applications; it can be used as monostable, astable multivibrators, DC to DC converters, digital logic probes, analogy frequency voltage regulators and time delay circuits.
The IC 555 timer is 8-pin IC and it can operate in free- running (Astable Multivibrator) mode or in one-shot (Monostable Multivibrator) mode. Pin configuration is as shown fig (1.). It can produce accurate and highly stable time delays or oscillations.

THEORY:

Astable Multivibrator often called a free-running Multivibrator. External Trigger input is not required to operate the 555 as an Astable Configuration. However, the time during which the output is either high or low is determined by two external components Resistor & Capacitor.
Fig (1) shows the 555 as Astable Multivibrator. Initially, when the output is high, capacitor C starts charging towards Vcc through resistor R_a and R_b. As soon as voltage across the capacitor equals to 2/3 Vcc, comparator-1 triggers the flip-flop, and the output is low. Now capacitor discharges through R_b and transistor Q_1. When the voltage across capacitor c equals to 1/3Vcc, comparator-2's output triggers the flip-flop, and the output goes high. Then the cycle repeats. The output voltage waveforms are as shown in fig (2).
In this way capacitor periodically charges discharges between 2/3Vcc and 1/3Vcc respectively.
The time during which the capacitor charges from 1/3Vcc to 2/3 Vcc is equal to the time, the output is high and is given by

$$tc = 0.69(Ra + Rb)\ C1$$

The time during which the capacitor discharges from 2/3 Vcc to 1/3Vcc is equal to the time, the output is low and is given by

$$td = 0.69(Rb)\ C1$$

The Total Time period of the pulse is the sum of charge time and discharge time, time period is given by

$$T = t_c + t_d$$

$$= 0.69(Ra + 2Rb)\ C1$$

This, in turn gives the frequency of oscillation as given below

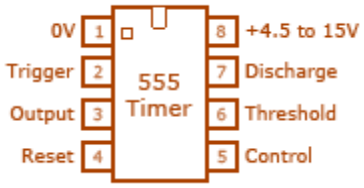
$$F = \frac{1}{T} = \frac{1.45}{(Ra+2Rb)C1}$$

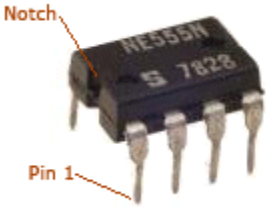
Duty Cycle: This term is in conjunction with Astable Multivibrator. The duty cycle is the ratio of the time t_c during which the output is high to the total time period T. It is generally expressed as a percentage.

$$\%\text{Duty cycle} = \frac{tc}{T} * 100$$

$$= \{\frac{Ra+Rb}{Ra+2Rb}\} * 100$$

Pin Diagram of 555 IC Timer





Astable Multivibrator:

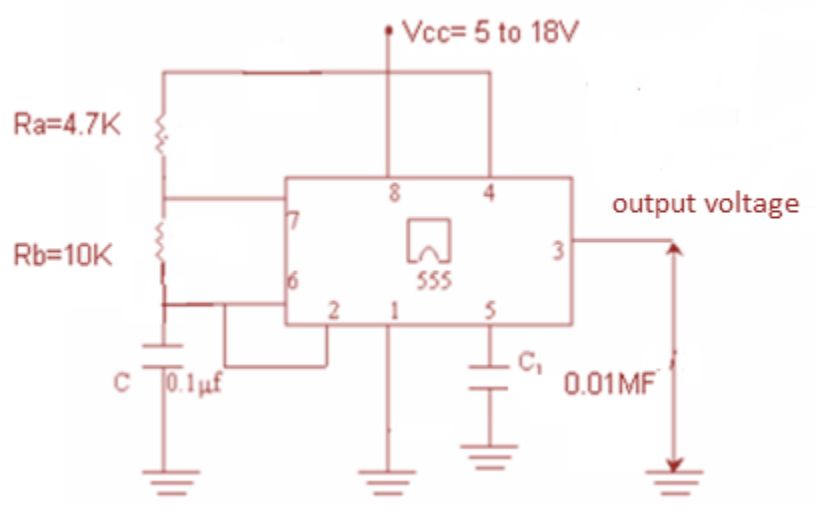


Figure 1

Tabular column

V_{CC}=_____

S. no	R_a	R_b	C	T_{on}		T_{off}		$T= T_{on} + T_{off}$		%Duty Cycle		Vopp (v) Squ	Vopp (v) Tri	$1/3V_{cc}$		$2/3V_{cc}$	
				Thero	Pract	Thero	Pract	Thero	Pract	Thero	Pract			Thero	Pract	Thero	Prac
1.																	
2.																	

V_{CC}=_____

S. no	R_a	R_b	C	T_{on}		T_{off}		$T= T_{on} + T_{off}$		%Duty Cycle		Vopp (v) Squ	Vopp (v) Tri	$1/3V_{cc}$		$2/3V_{cc}$	
				Thero	Pract	Thero	Pract	Thero	Pract	Thero	Pract			Thero	Pract	Thero	Prac
1.																	
2.																	
3.																	

PROCEDURE:

1. Connect the IC 555 timer as an astable configuration as shown in fig (1)
2. Connect the C.R.O at the output terminals.
3. Give the supply voltage to pin 8 in circuit based on desired charging voltage.
4. Record & observe the waveforms at the output terminals and also across the capacitor.
5. Verify with the Sample output waveforms as shown in fig (2)
6. Calculate Tc, Td, time period of pulse (T) and duty cycle percentage theoretically and verify with practical values.
7. Find the charging time t_c discharging time t_d and totals time period T from the output waveform.

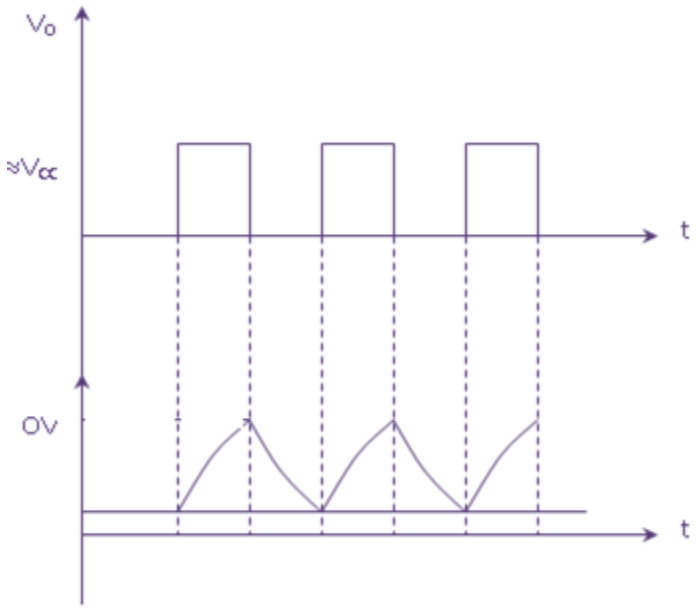
8.Verify these values with theoretical values and calculate the % of the duty cycle.

Where $T_c = 0.69 (R_B + R_A)C$, $R_A = R_2 + R_1$

$T_d = 0.69 R_B C$

$T = Tc + T_d$ % of Duty Cycle = $\{\frac{tc}{T}\}$ * 100

WAVEFORMS:



DISCUSSION OF RESULT:

Students will be able to observe & discuss

1. Astable multivibartor waveforms and discuss 555 timer IC specifications
2. Change of duty cycle when capacitor C1 is changed
3. Change of output amplitude when Vcc for 555 IC is changed

PRELAB QUESTIONS:

1. What are the important features of the IC555 Timer.
2. Define Duty cycle.
3. What are the modes of operation of Timer and state the difference between two operating modes of the 555 Timer.
4. Why do we connect pin 4 of IC 555 timer to supply
5. What is the function of control input (pin5) of 555 timer?

Experiment no:3

MULTIPLEXER-LOGIC REALIZATION & PARALLEL TO SERIAL CONVERSION

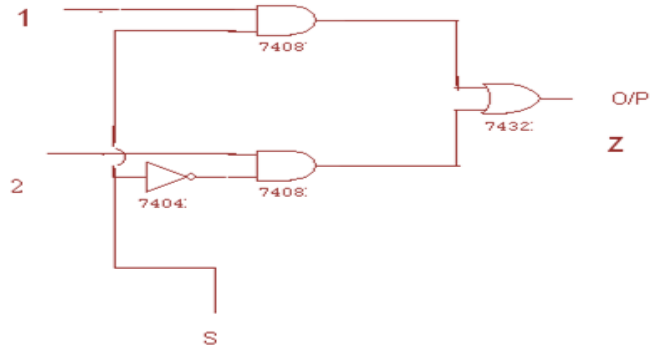
AIM: 1.To study and design 2:1 MUX using logic gate realization
2. To design 8:1 MUX as parallel to serial conversion using 74151 IC.
3. To implement a Boolean function using 8:1 MUX

EQUIPMENTS & COMPONENTS: 1. Digital IC Trainer kit
2. Bread Board
3. Multimeter
4. Connecting patch chords.
5. +5 V fixed power supply
6. ICs 7408, 7432, 7404,74151
7. Single stand wires

THEORY: Multiplexer is a combinational circuit it selects one out of several inputs and gives single output. It is also known as data selector used to gate out one out of several inputs which is controlled by a set of selected inputs. It can also be used for parallel to serial conversion

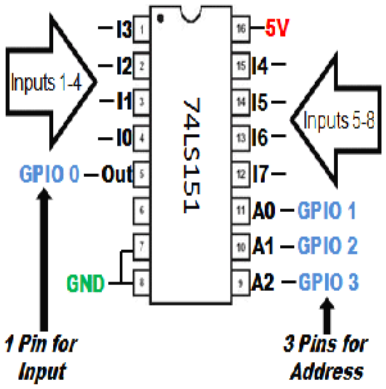
PROCEDURE:
1. Connect the circuit of 2: 1 Mux as shown in figure (1)
2. Connect +Vcc and GND to each logic gate
3. Verify the truth table
4. Using MUX IC design for required Boolean function figure (2)

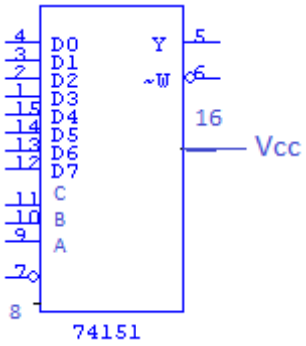
TWO INPUT MUX USING LOGIC GATES



Select Input	Output
0	$Z=I_2$
1	$Z=I_1$

PIN DIAGRAM OF 8:1 MUX(74151)

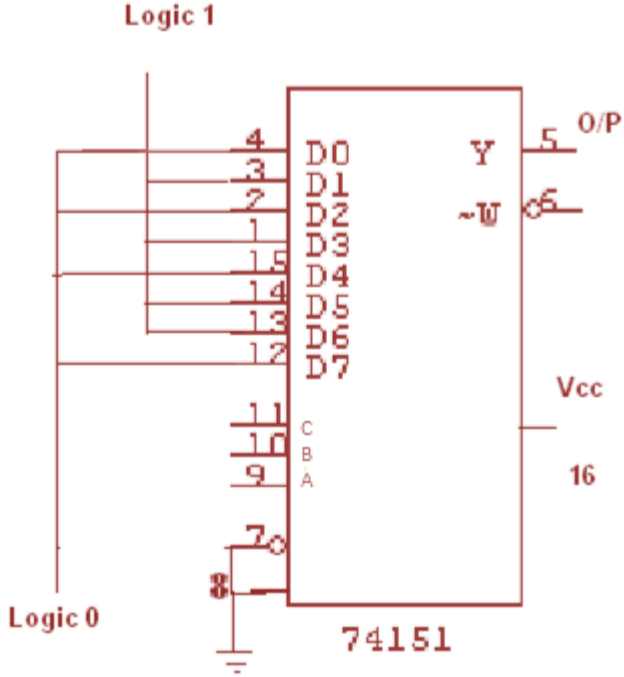




D0 – D7 -------→ Data inputs
ABC -------→Select lines
Vcc -------→ +5V
Strobe ----→ Connect to Gnd
Y--→ out put , W --→ complement output

IMPLEMENTATION OF BOOLEAN FUNCTION

F(A,B,C)= ∑ m (1,3,5,6)



INPUTS			OUTPUTS
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

DISCUSSION OF RESULT:

Students will be able to observe

1. Implementation of a Boolean function using logic gates & Mux I.C

2. Change in the digital output for various select line changes.

PRELAB QUESTIONS:

1. State difference between Demux & Decoder
2. Applications of Mux & Demux
3. State difference between encoder & Mux

Experiment no:4

TRIANGULAR, SQUARE & SINE WAVE GENERATOR

AIM: 1 To study the operation of triangular wave generator and Design for different frequencies
2. Compare the theoretical and practical frequencies for different RC Combinations

EQUIPMENTS & COMPONENTS:
1. IC Trainer Kit / Bread board
2. Multimeter
3. C R O & probes.
4. ± 15 V Power supply
5. D.C.B
6. IC 741(2 nos)
7. Resistors 10 K (2 nos)
8. 50K Pot
9. Capacitors 0.047µ F, 0.01µ F
10. Patch chords/connecting wires

THEORY: Figure 1 shows the triangle wave generator using op-amp. The generator consists of a comparator A 1 and an integrator A2. The comparator A 1 compares the voltage at point P continuously with the inverting input that is at 0V. When the voltage at P goes slightly below or above 0V, the output of A 1 is at the negative or positive saturation level, respectively. To illustrate the circuit's operation, let us set the output of A 1 at positive saturation +V sat. This +V sat of A 1 and the other is the negative-going ramp of A2. When the negative-going ramp attains a certain value –V ramp, point P is slightly below 0V; hence the output of A 1 will switch from output of A2 will now stop going negatively and will begin to go positively. The output of A2 will continue to increase until it reaches +V ramp. At this time the point P is slightly above 0V; therefore, the output of A 1 is switched back to the positive saturation level +V sat. The sequence then repeats. The output waveform is as shown in figure 2

The frequencies of the square wave and the triangular wave are the same and is given by fo = R3/(4R1C1R2) where fo = Output frequency
R1= 10K, R2= 10K

R3= 40K (Pot variable)

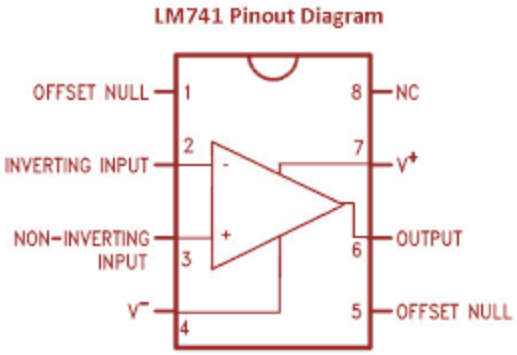
C=0.047µF/ 0.01µ F/0.3 µ F/0.4 µ F

Triangular Vpp =$2*\frac{R2}{R3} * V_{Sat}$ V_{Sat} =14v or 15v

Square wave Vpp =$2*V_{Sat}$

PROCEDURE:

1. Connect the circuit as shown in figure (1)
2. Adjust the pot for desired (40K) ,diodes are optional
3. Connect ± 15 V supply to both the 741 ICs
4. connect channel 1 of CRO at the output of A1 and channel 2 at output of A2
5. Plot the wave forms noting the frequency and amplitude in tabular column



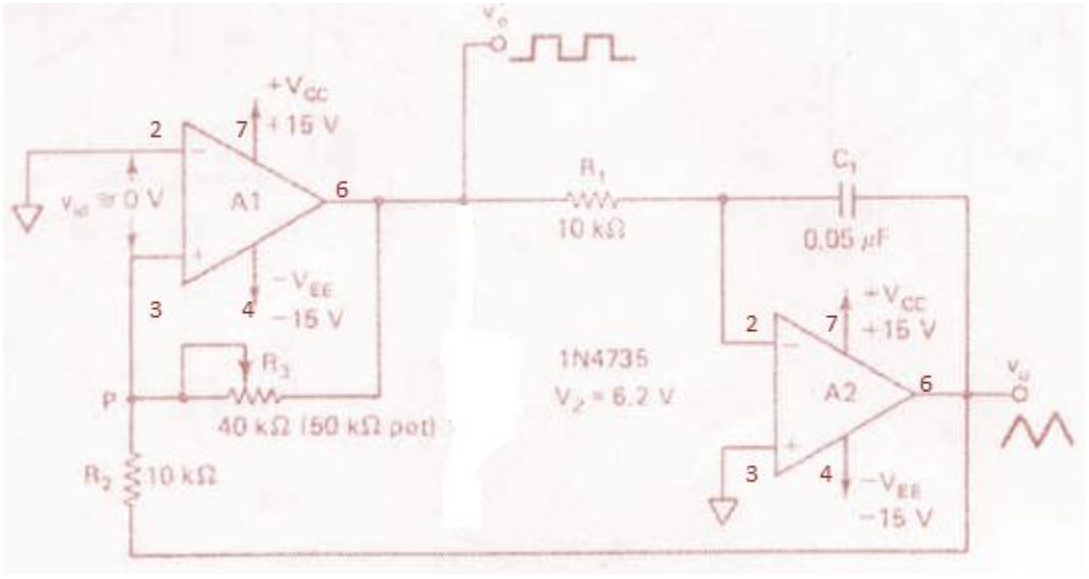


Figure 1

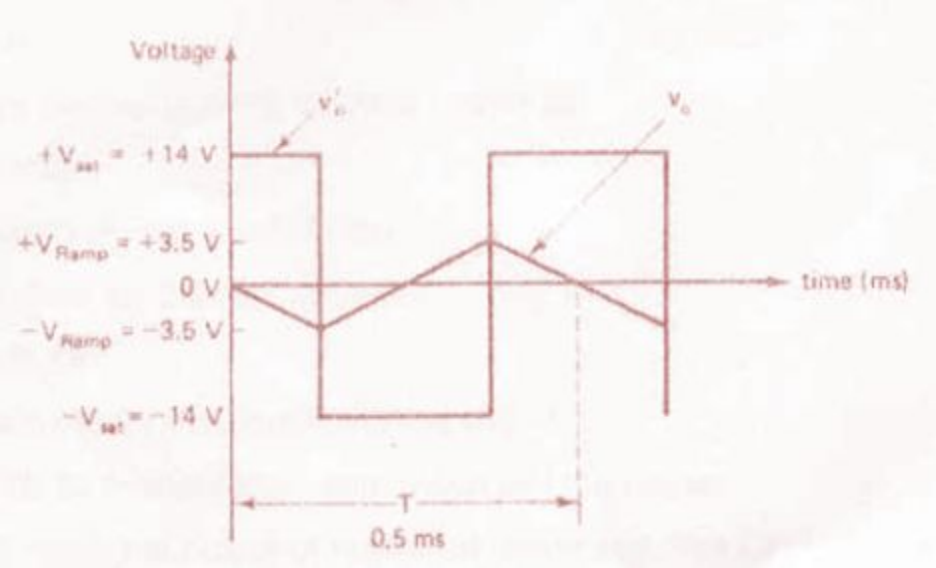


Figure 2

TABULAR COLUMN:

Sl no	R	C	Frequency(Hz)		Amplitude(V)			
					Square		Triangular	
1.	40K	0.3µF	Thero	pract	Thero	pract	Thero	pract
2.	40K	0.4µF						
3.	20K	0.3µF						
4.	20K	0.4µF						
5.								

SINE WAVE GENERATOR (wein-bridge oscillator)

Theroy: A basic wein bridge oscillator is shown using opamp.Diodes (4148)across feedback resistor are used to maintain constant output voltage.A 47KΩ dual potentiometer is used to vary the frequency for limited range.10 turn trim pot helps to adjust the gain at high resolution capacitor 0.1 µF and couples the signal to the next section.

Design:

Gain required for sustained oscillation is $A_v = 1/\beta = 1.45$

(PASS BAND GAIN) (i.e.) $A_v = 1+R_f/R_1 = 1.45$ Let Rf =10k

$\therefore R_1 = 22k$

Frequency of Oscillation $f_o = 1/2\pi R C$

Given $f_o = 1$ KHz

Let C = 1KpF

$\therefore R = 1/2 \pi f_o C$

PROCEDURE:

1.Connect the circuit as shown in figure (3)
2.Switch on the power supply and CRO.
3.Note down the output voltage at CRO.
4.Plot the output waveform on the graph.
5.Redesign the circuit to generate the sine wave of frequency 2KHz.
6.Compare the output with the theoretical value of oscillation

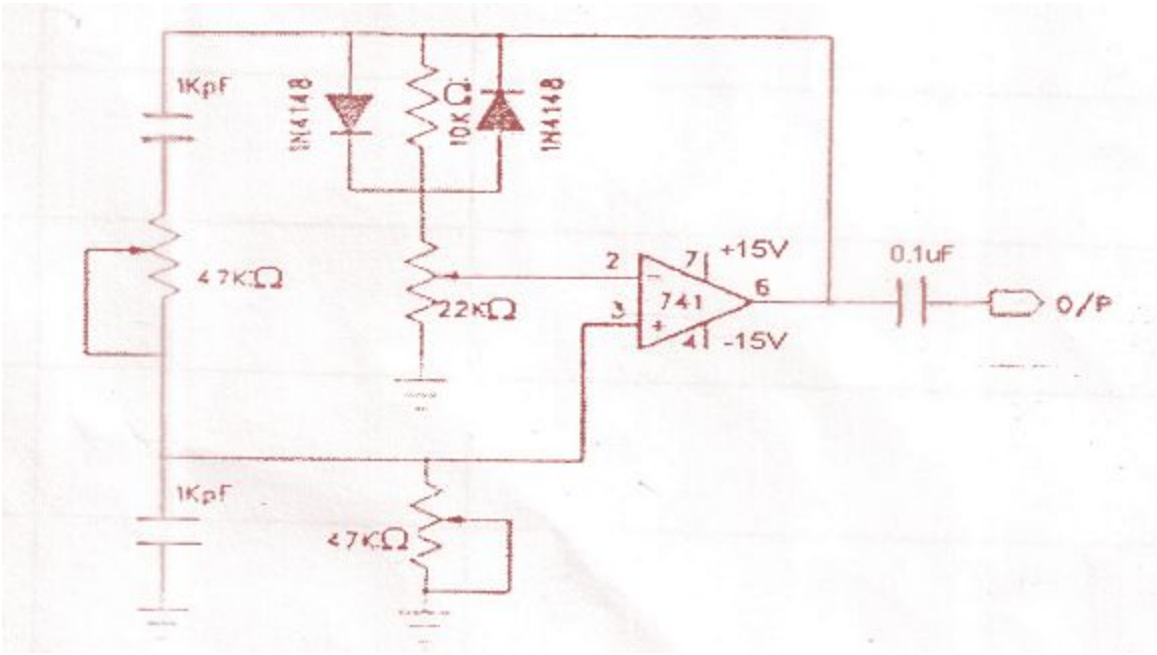
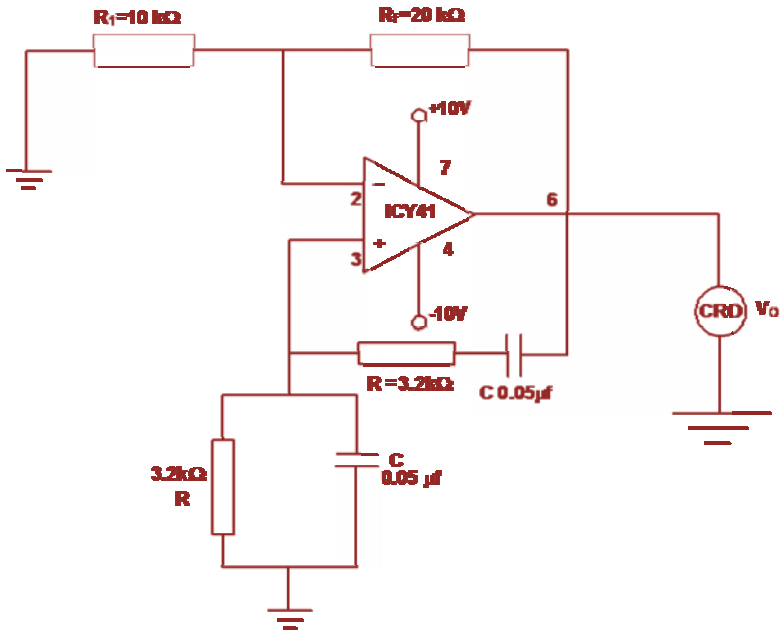
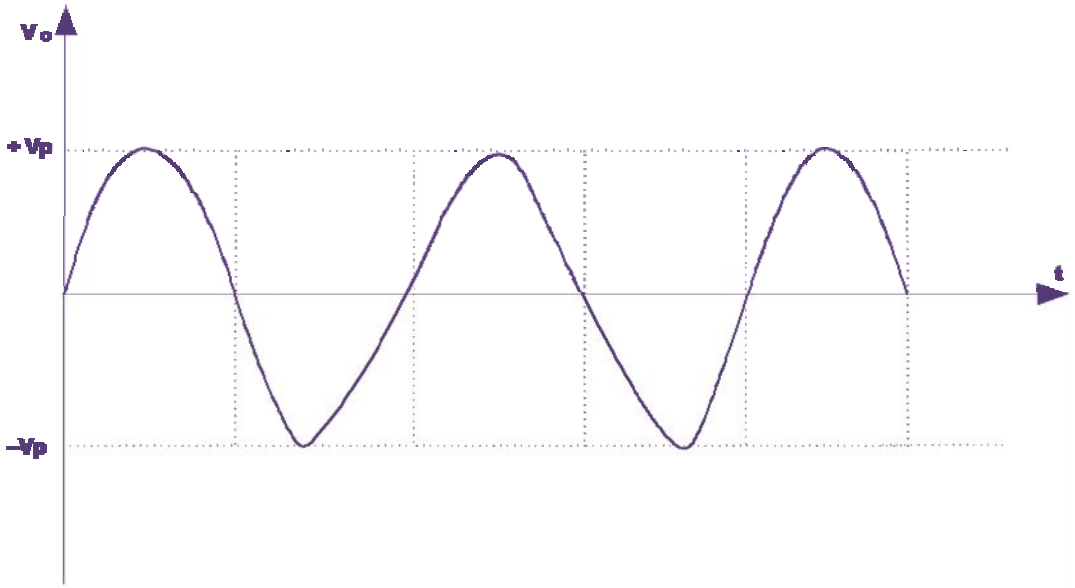


Figure 3





Equations: Wein Bridge Oscillator

Closed loop gain $A_v = (1+R_f/R_1) = 3$
Frequency of Oscillation $f_0 = 1/(2\pi RC)$

Observation:

Peak to peak amplitude of the output = Volts.
Frequency of oscillation = Hz

Sl no	R	C	Frequency(Hz)		Amplitude (ppV)	
			Theoretical	Practical	Theoretical	Practical
1.						
2.						
3.						
4.						

DISCUSSION OF RESULT:

Students will observe

1. Change in amplitude of generated square wave & triangular wave when V_{sat} and resistors R_2 & R_3 are varied.
2. Change in frequency of generated square wave & triangular wave with varied capacitor C_1 varied.
3.For sine wave changing the component values of R1 &C1 Will change frequency & Rf & R1 will vary amplitude or gain

PRELAB QUESTIONS:

1. Do we require any input signal for a square wave generator give reason
2. What is the combination of OP-AMP circuits used for generation of Triangular wave generator?
3. What is the O/P of Integration if positive unit step signal is applied?
4. Define Comparator circuit.
5. What are the applications of Square & Triangular wave generator circuit?
6. How can we increase the amplitude of the o/p square and triangular wave?
7. State the two conditions for oscillations.
8. Define an oscillator?
9. What is the frequency range generated by Wien Bridge Oscillator?

Experiment no:5

ADDERS & SUBTRACTORS-REALIZATION OF COMBINATIONAL LOGIC

AIM: 1 To study and design Half &Full i) Adders ii) Subtractors Using combinational Logic gates

EQUIPMENTS & COMPONENTS: 1.. IC Trainer Kit / Bread board
2. Multimeter
3. 5 V Power supply
4. IC 7486(EX-OR), IC 7404 (NOT)
5. IC 7408 (AND)
6. IC 7432 (OR),
8. Single stand wires

THEORY: Half adder is addition of two Boolean Inputs. Used to add two logical inputs A and B. getting the output in sum and carry. Then the Boolean equation for which output '1' is written in sum of product form. Which becomes easier to implement the circuit. Similarly for a half subtractor we get two outputs difference & borrow Full adder or subtractor has three inputs A ,B,C and only two outputs as shown in below circuits

PROCEDURE: 1. Connect the circuit of half adder using digital trainer kit

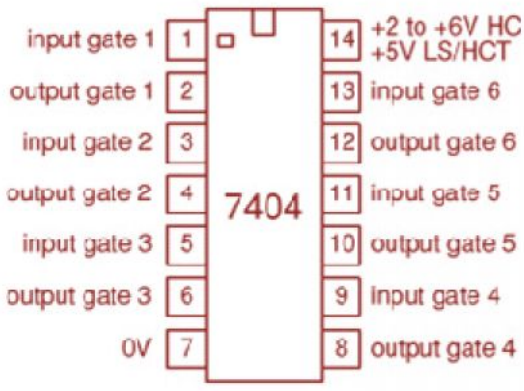
2.Connect Vcc and GND for each IC used in circuit

3. Verify the truth table for sum and carry

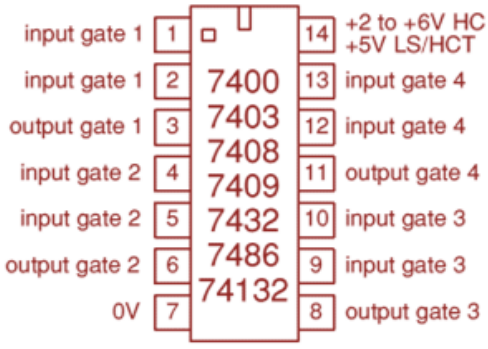
4. Repeat same for full adder, half subtractor & full subtractor

PIN DIGARMS

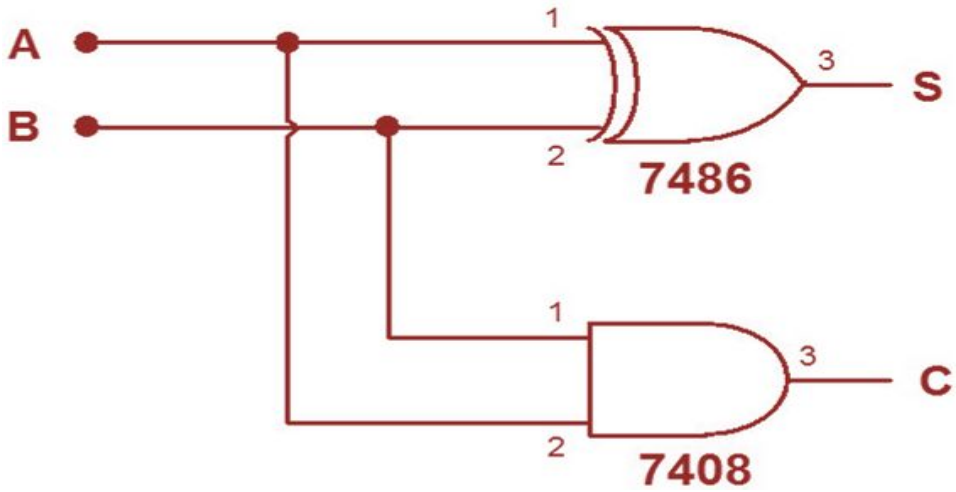
NOT Gate



NAND/AND/EX-OR Gate



HALF ADDER

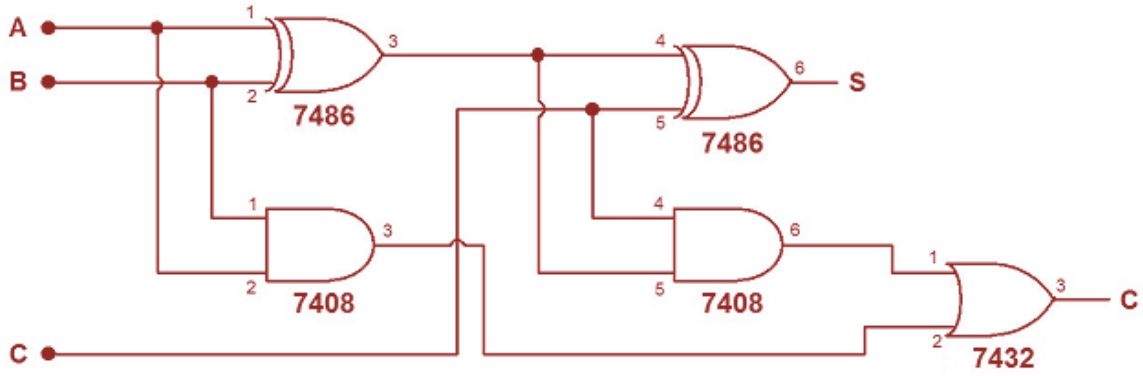


Truth table of half adder:

Sum = S = A' B + A B '
Carry = C = A B

INPUTS		OUTPUTS	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

FULL ADDER



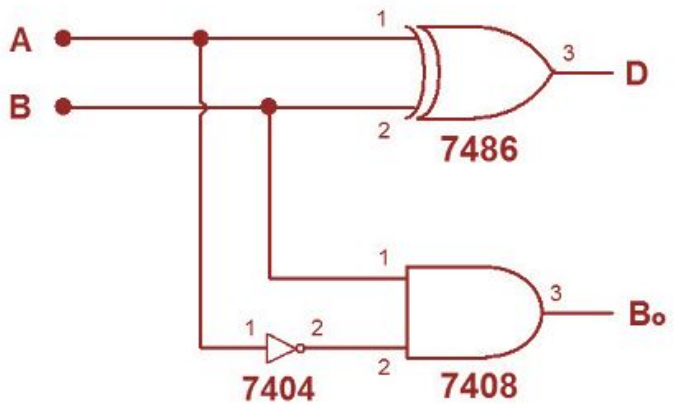
Truth table for Full adder:

INPUTS			OUTPUTS	
A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Sum = S = A' B' C + A B' C + A' B C + A B C

Carry = C = A' B C + A B C ' + A B C

HALF SUBTRACTOR



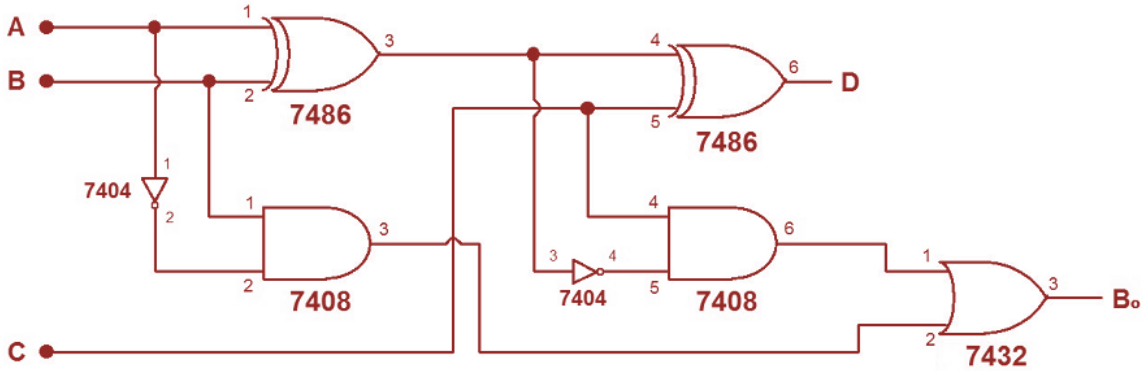
INPUTS		OUTPUTS	
A	B	D	Bo
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Truth table for Half Subtractor:

Difference = D = A' B' + A B'

Borrow = Bo = A' B

FULL SUBTRACTOR



Truth table for Full Subtractor:

Difference = D = A' B' C + A B' C + A B' C ' + A B C
Borrow = Bo = A' B' C + A B' C + A' B C + A B C

INPUTS			**OUTPUTS**	
A	B	C	DIFFERENCE	BORROW
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

DISCUSSION OF RESULT: Students will observe implementation of

1. Half & full adders, subtractor using combinational logic gates.
2. Half adders full adder Using universal gates

PRELAB QUESTIONS:
1. How can we Implement sum of half adder using only one 7400 IC?
2. How can we Implement a Not gate using only Nand gates?
3. What are universal gates? why are they called so?

Experiment no:6

CLIPPERS & CLAMPERS USING OP-AMPS

AIM: 1.Study the operation of various types of clippers and clampers like positive, Negative using operational amplifier 741
2. Plot output waveforms for sine wave input at different levels

EQUIPMENTS & COMPONENTS: 1.Clippers& Clampers kit / bread board
2. Multimeter
3. Function generator
4. C R O & probes.
5. ± 15 V Power supply
6. IC 741
7. Patch chords

THEORY: Clipper is a circuit that removes positive or negative level of the input signal and can be designed using op amp with rectifier diodes. The op amp is basically used as a voltage follower with the feedback path ,the reference voltage determines the level of voltage to be clipped both either positive or negative . A negative clipper is obtained by just reversing the diode
Clamper is a circuit used to add D.C voltage to the input signal .It is also called a D.C inverter or restorer

PROCEDURE:

1. Connect the trainer to mains and switch on the power supply
2. Measure the output voltage of regulated power supply i.e. +12V and -12V using digital multimeter
3.Observe the output of the on board signal generator with the help of Oscilloscope Signal should be sine wave of 1KHZ frequency with 10Vpp amplitude or connect external signal generator

Positive clippers

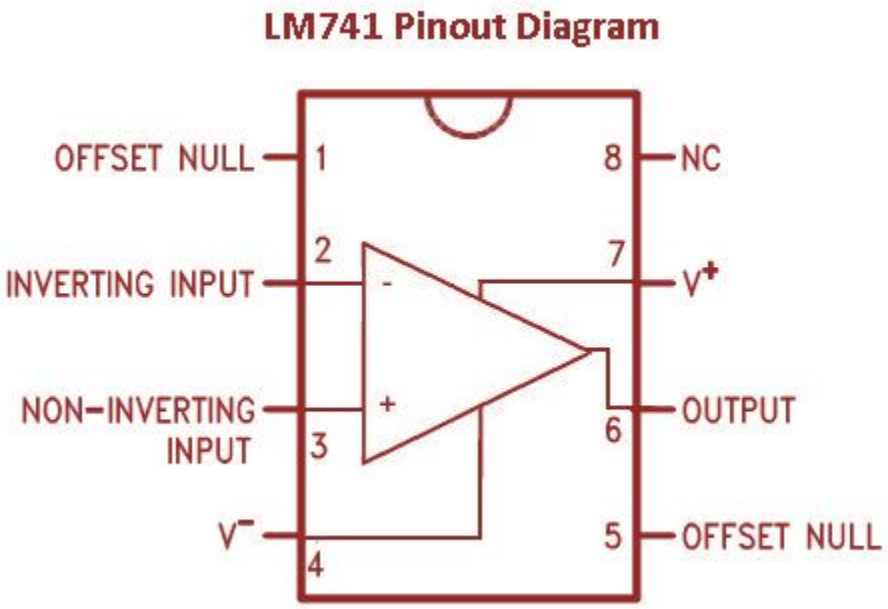
4. Connect the circuit as shown in fig.(1)
5. Observe the input and output waveforms with the help of dual trace Oscilloscope and compare them with the expected waveform
6. Repeat the same at different voltage source by varying 10 K pot
7. Now connect a negative V ref fig.(2) and observe the wave forms

Negative clippers

8. Connect the circuit as shown in fig.(3)
9. Observe the input and output waveforms with the help of dual trace Oscilloscope and compare them with the expected waveform
10. Repeat the same at different voltage source and positive Vref fig.(4)

Positive clampers

11. Connect the circuit as shown in fig.(3)
12. Observe the input and output waveforms with the help of dual trace Oscilloscope and compare them with the expected waveform
13. Repeat the same at different voltage source and changing the Vref



Positive clipper circuit with waveforms for positive V ref

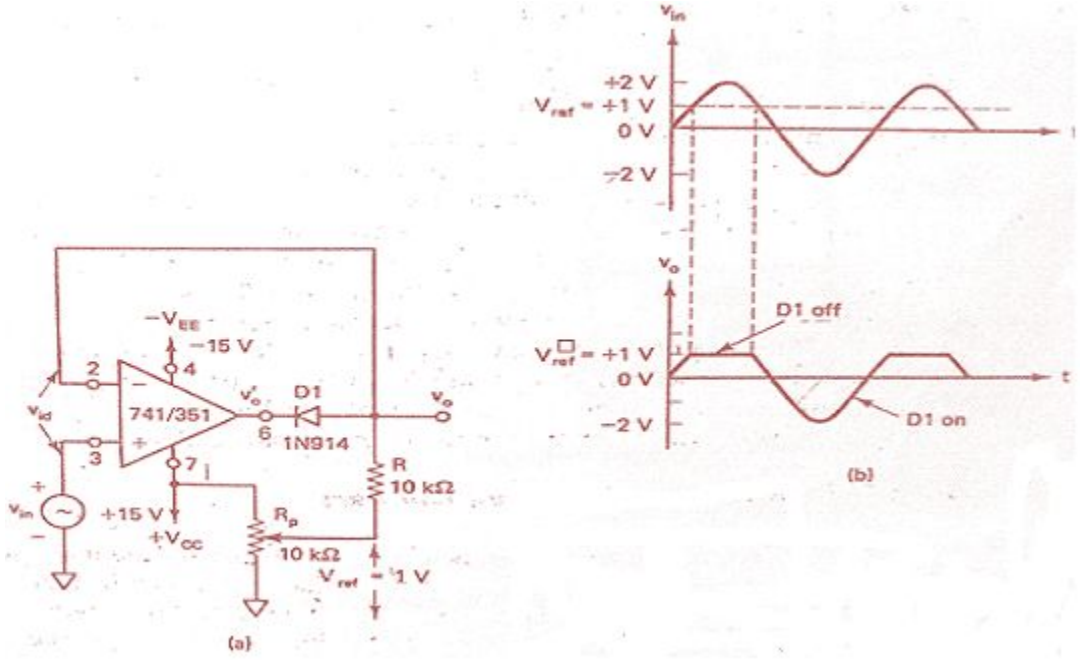


Figure 1

Positive clipper circuit with waveforms for negative V ref

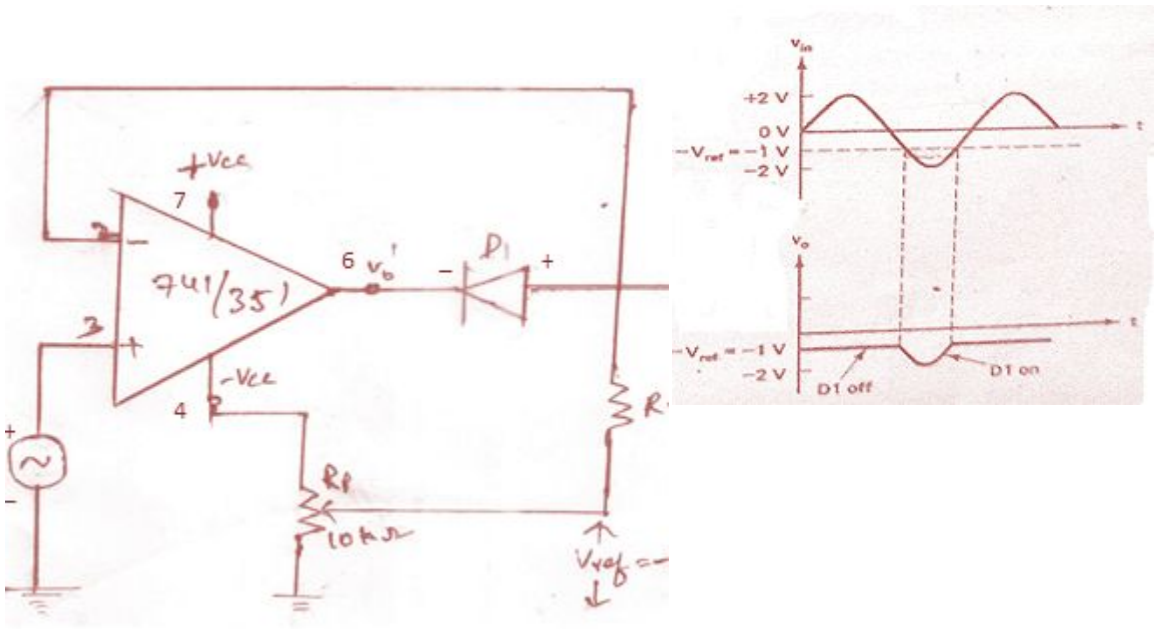


Figure.2

Negative Peak clipper with negative V ref wave forms

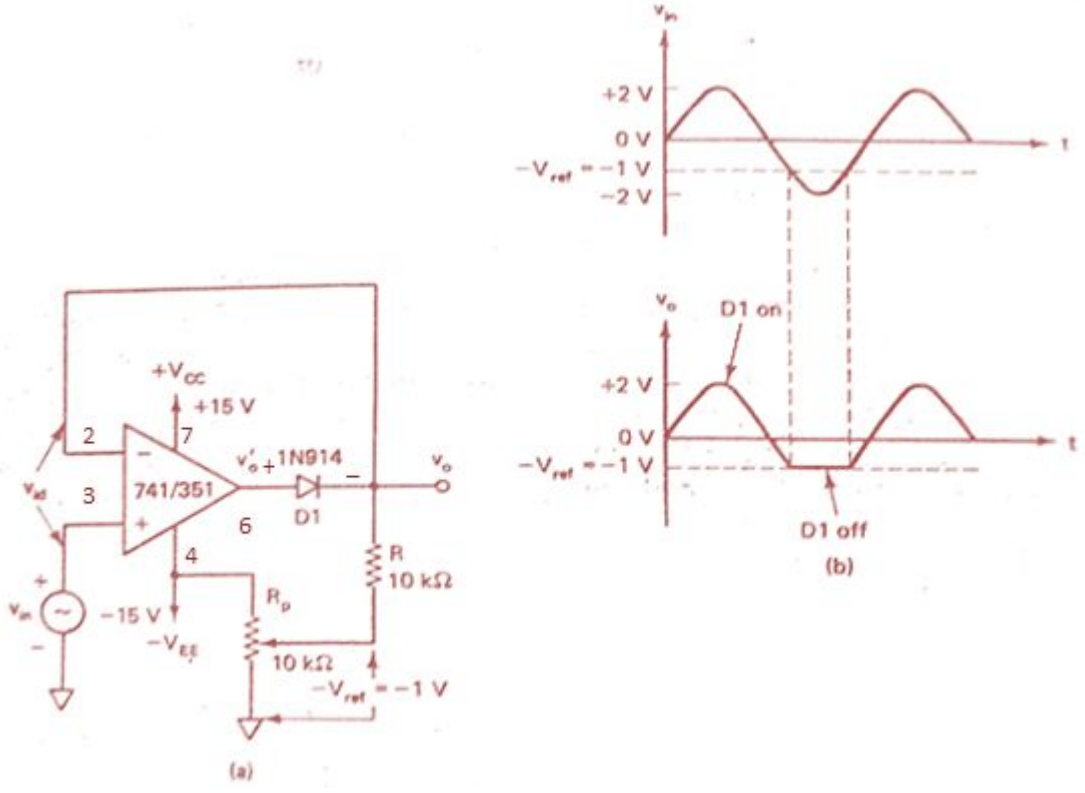


Figure 3

Negative Peak clipper with positive Reference

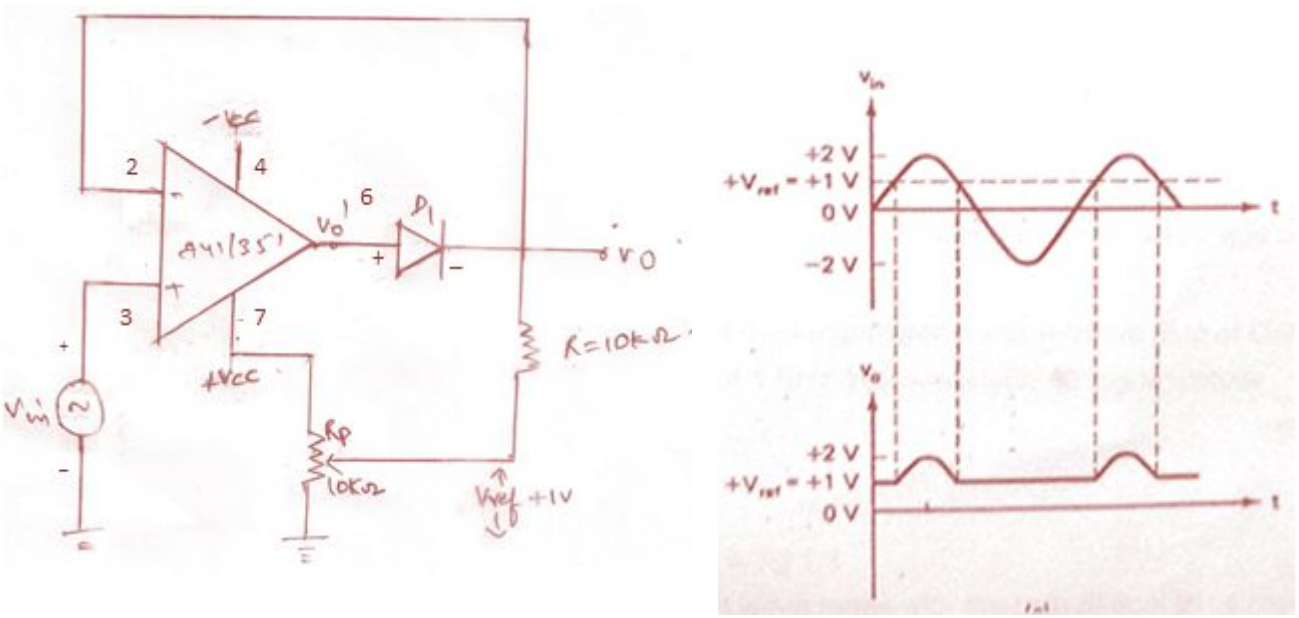
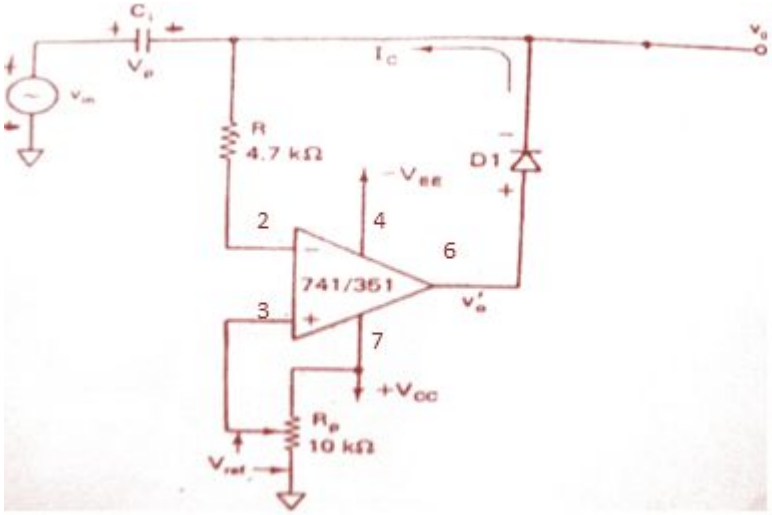


Figure 4

Clippers

S.no	Type of Clipper	V_{in}(p-p)	V_0(p-p)	$V_{0\ RMS}$ (Multimeter)
1.	Positive clipper with positive V_{Ref}			
2.	Positive clipper with negative V_{Ref}			
3.	Negative clipper with positive V_{Ref}			
4.	Negative clipper with negative V_{Ref}			

Positive Clamper with waveforms



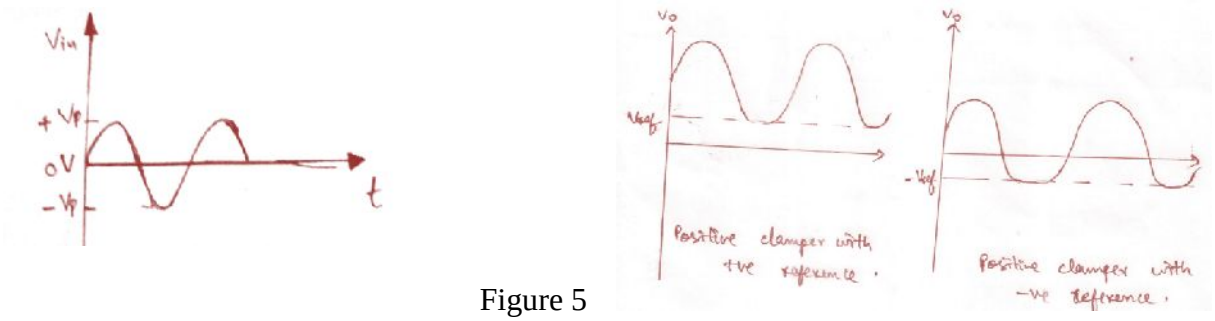
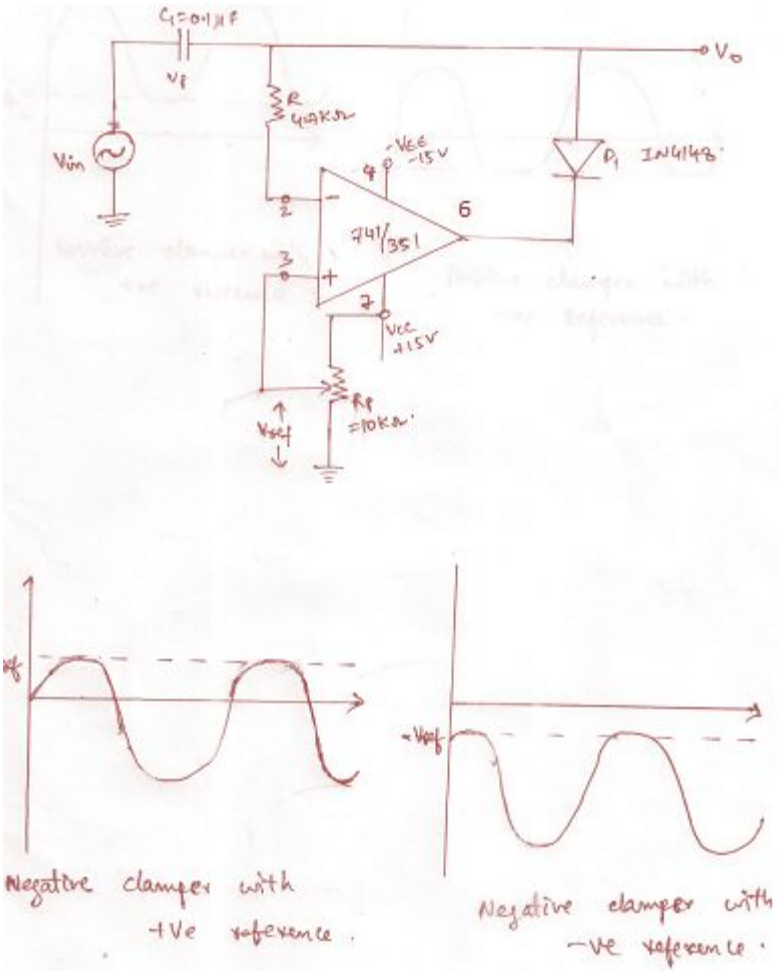


Figure 5

Negative Clampers with waveforms



S.no	Type of Clamper	V_{in}(p-p)	V_0(p-p)	$V_{0\ RMS}$ (Multimeter)
1.	Positive Clamper with positive V_{Ref}			
2.	Positive Clamper with negative V_{Ref}			
3.	Negative Clamper with positive V_{Ref}			
4.	Negative Clamper with negative V_{Ref}			

DISCUSSION ON RESULT: Students will observe that

1. As the reference voltage through Pot changes the clipping & clamping limit of wave changes
2. Polarity of diode position will decide positive or negative clipper & clamper
3. Positive or negative Vref of clipper or clamper is decided by DC biasing voltage connected to biasing pins of op amps

PRELAB QUESTIONS:

1. Why clamper is called a DC restorer?
2. What are the applications of clippers and clampers?
3. What is the factor which determines clipping level in a clipper?

Experiment no:7

DESIGN OF INTEGRATOR & DIFFERENTIATOR

AIM: 1. To design and demonstrate the operation of a practical Differentiator & Integrator using op-amp
2. To plot differentiated and integrated outputs for different input waveforms

EQUIPMENTS & COMPONENTS:

1. Digital IC Trainer kit / bread board
2. Multimeter
3. Function generator
4. C R O & probes.
5. ± 15 V Power supply
6. IC 741
7. Resistors 4.7K,10 K
8. Capacitors 0.01µ F
9. Single Stand Wires
10. Decade Capacitance .Box
11. Decade Resistance .Box

THEORY:

Integrator: A circuit in which the output voltage is the integration of the input voltage is called an integrator**.** In the practical integrator to reduce the error voltage at the output, a resistor R_F is connected across the feedback capacitor C_F.

$$V_o = -\frac{1}{R_1 C_f} \int V_{in}\, dt$$

Thus, R_F limits the low-frequency gain and hence minimizes the variations in the output voltage.

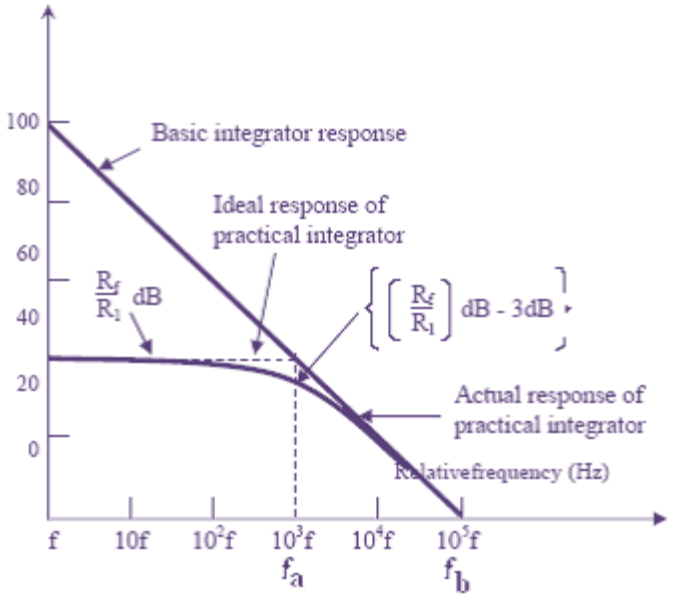


Figure1 :Frequency response of integrator

The frequency response of the integrator is shown in the above fig. f_b is the frequency at which the gain is 0 dB and is given by $f_b = 1/2\pi R_1 C_f$.

In this fig. there is some relative operating frequency, and for frequencies from f to f_a the gain R_F/R_1 is constant. However, after f_a the gain decreases at a rate of 20 dB/decade. In other words, between f_a and f_b the circuit of fig. 2.1 acts as an integrator. The gain-limiting frequency f_a is given by $f_a = 1/2\pi R_f C_f$. Normally $f_a<f_b$. From the above equation, we can calculate R_f by assuming f_a & C_f. This is very important frequency. It tells us where the useful integration range starts. If $f_{in} < f_a$ - circuit acts like a simple inverting amplifier and no integration results, If $f_{in} = f_a$ - integration takes place with only 50% accuracy results, If $f_{in} = 10f_a$ - integration takes place with 99% accuracy results. In the circuit diagram of Integrator, the values are calculated by assuming f_a as 50 Hz. Hence the input frequency is to be taken as 500Hz to get 99% accuracy results.

Design Aspects for Integrator: Design for a practical circuit with D.C gain of 20 to integrate a signal of maximum frequency 2KHz.

Steps For Design:

1.The D.C gain for the practical integrator is $|A|_{dc} = \frac{Rf}{R_1}$. Choose R_f=100KΩ ∴ R_1=5 KΩ (use R0=4.7KΩ)

2. Condition for Proper integrator I/P frequency $f > 10f_a$.

$f_a \rightarrow$ break frequency. ∴ $f/f_a = 10 \Rightarrow f_a = 200$ Hz.

$f_a = 1/2\pi R_f C_f$.

Choose C_f=0.01μf. ∴R_f=79.5 KΩ. (use R_f=100KΩ)

NOTE: For $f < f_a$ circuit behaves as an inverting amplifier & output

$$V_0 = R_f/R_1 . V_{in}.$$

For $f > f_a$ circuit in an integrator & output $V_o = 1/R_1C_1 \int V_{in}\, dt$.

Differentiator:

As the name suggests, the circuit performs the mathematical operation of differentiation, i.e. the output voltage is the derivative of the input voltage.

$$Vo = - Rf\ C1 \frac{dVin}{dt}$$

Both the stability and the high-frequency noise problems can be corrected by the addition of two components: R1 and Cf, as shown in the circuit diagram.

This circuit is a practical differentiator. The input signal will be differentiated properly if the time period T of the input signal is larger than or equal to RfC1. That is, T>= RfC1

Differentiator can be designed by Selecting fa equal to the highest frequency of the input signal to be differentiated. Then, assuming a value of C1<1 F, calculate the value of Rf . Calculate the values of R1and Cf so that R1C1=RfCf.

Design Aspects For Differentiator: Design for a practical differentiator circuit that will differentiate an Input signal with maximum frequency 2 KHz.

Steps For Design:

1. Choose $f_a=f_{max}=2kHz$.
2. Choose $C_1=0.01\mu f$. Now $f_a=1/2\pi Rfc1$ $R_f=1/2\pi RfC1=7.9K\Omega$ (use 10 KΩ).
3. Now $f_b=2f_a$ ($\therefore f_a<f_b$) & $R_1C_1=R_fC_f$ $f_b=1/2\pi RfC1$

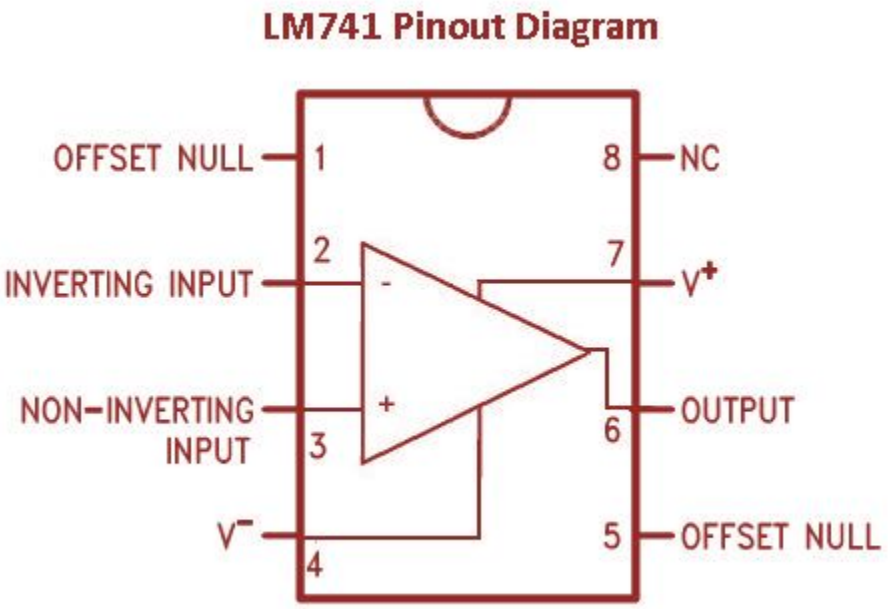
$\therefore R_1=3.9K\Omega$ (use 4.7KΩ)& $R_1C_1=R_f$

$\therefore C_f=5$ nf.

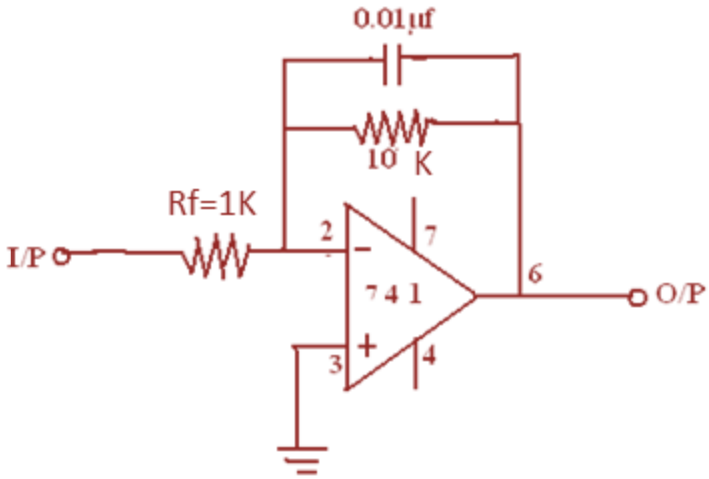
PROCEDURE:

1. Connect the integrator circuit as per design. Adjust the function generator to produce 2 volts P/P sine wave of 1 KHz.
2. Observe input & output simultaneously on the CRO. Measure & record the peak value of V_o & the phase angle of V_o with repeat V_i.
3. Repeat step (2) while increasing the frequency of I/P signal. Find the maximum frequency at which circuit performs integration. Compare with calculated value of f_a.
4. Now set function generator to 2V P/P square wave of 1 KHz to get the O/P of a triangle waveform. Plot the amplitude & frequency on a graph sheet
5. Similarly connect differentiator circuit verify that for inputs of sine wave and square wave we get outputs of cosine wave & spike wave respectively

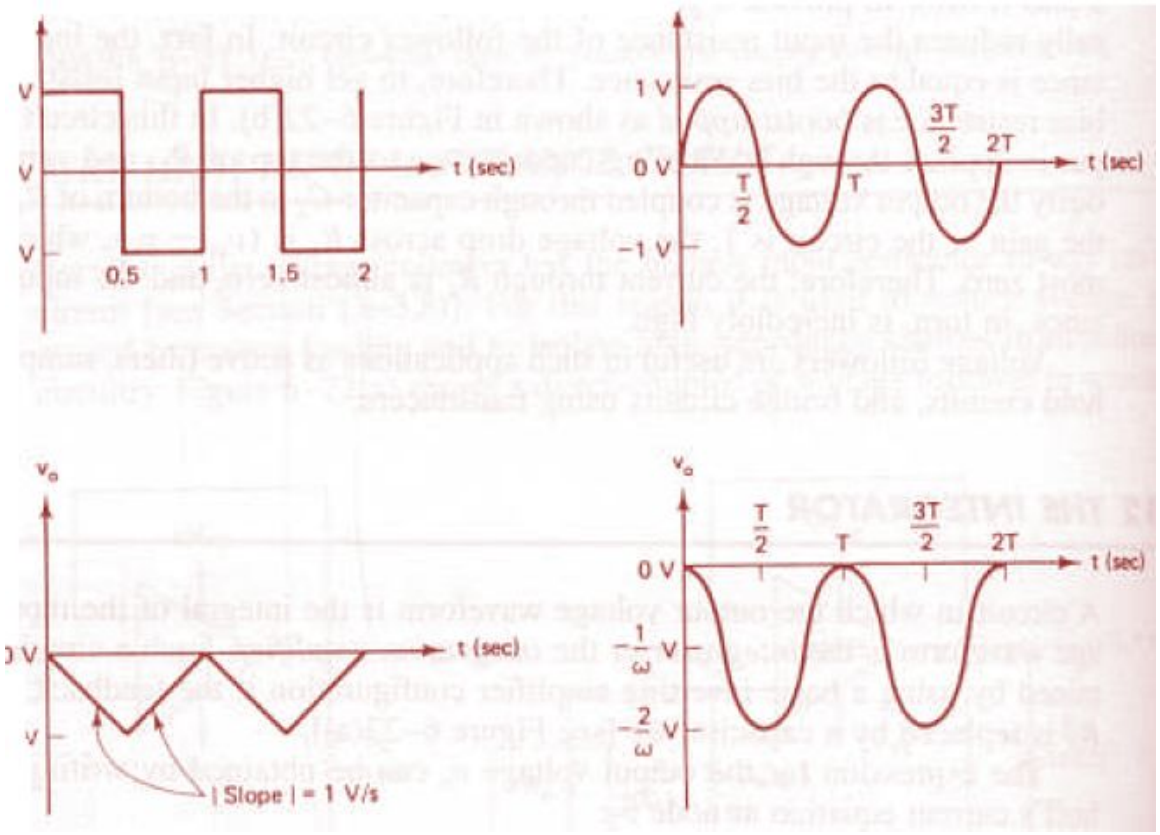
NOTE: The O/P amplitude of differentiator is directly proportional to the I/P frequency



Integrator Circuit



Practical integrator wave forms



fig(a)Square wave input resulting in triangular wave output

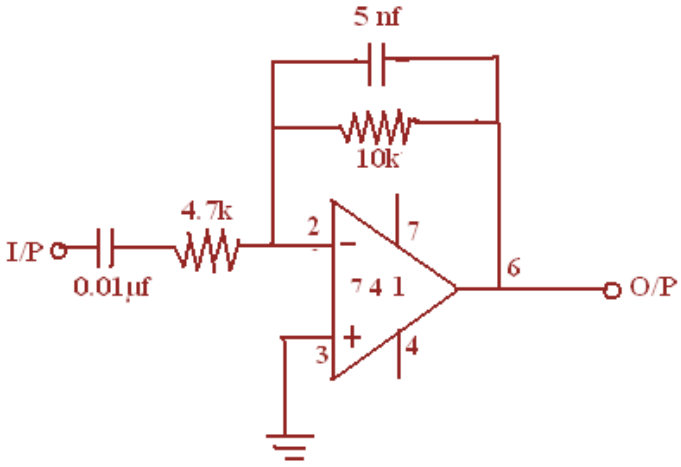
fig(b) Sine wave input resulting in cosine output

Input Frequency=-----

Phase angle θ $= \frac{\text{Time delay between input \& } output\ sine\ or\ cosine\ waveforms(td)}{\text{Total time periodof input sine wave(T)}} * 360°$

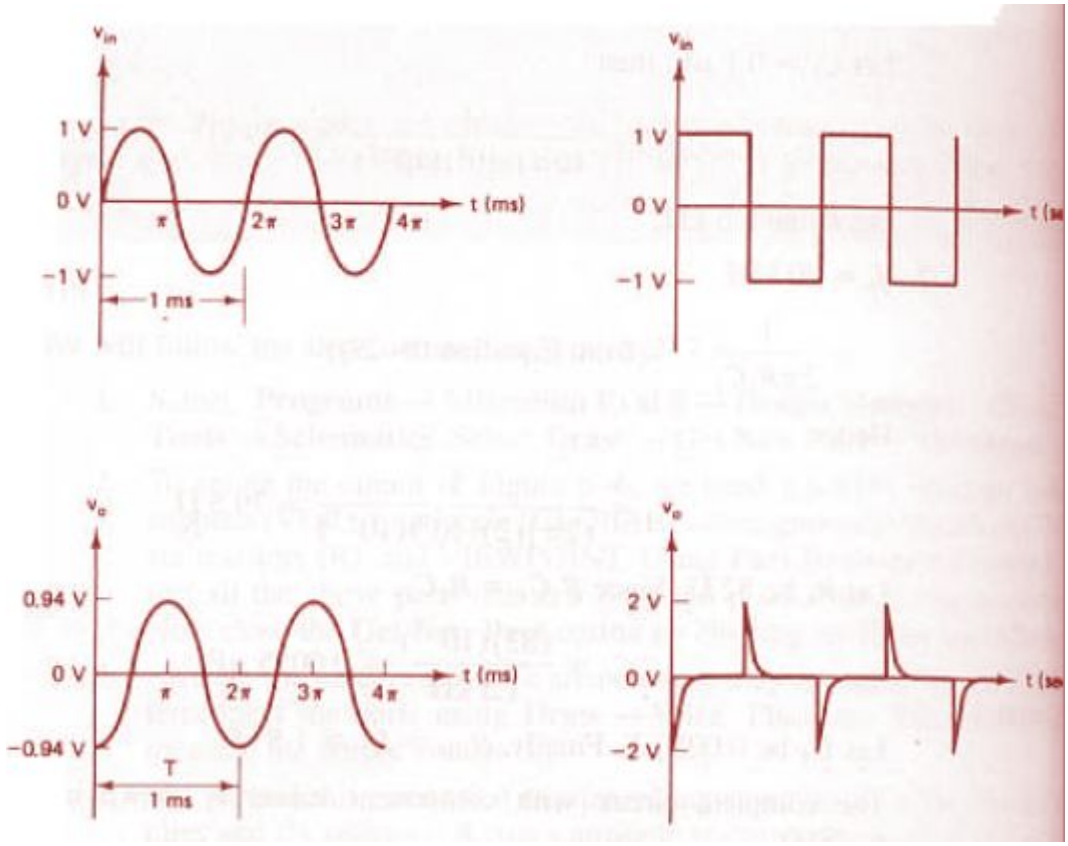
S.no	Input type	V_{in}(pp)	F_{in}(kHz)	V_o(pp)	F_{out}(kHz)	Phase angle (θ)
1.	Sine Wave					
2.	Square Wave					

Differentiator Circuit



Expected waveforms

Practical differentiator



fig(a)Sine wave input resulting in cosine wave output

fig(b)Square wave input resulting in spike wave output

S.no	Input type	V_{in}(pp)	F_{in}(kHz)	V_o(pp)	F_{out}(kHz)	Phase angle (θ)
1.	Sine Wave					
2.	Square Wave					

DISCUSSION ON RESULT: Students will be able to observe

1. Practical integrator response changes for maximum frequency design F max with respect to Feedback resistor Rf
2. Practical Differentiator response depends on resistor R1 & capacitor Cf.
3. As input frequency is increased in integrator output voltage decreases and in differentiator output voltage increases

PRELAB QUESTIONS:

1. What are the Ideal characteristics of an op amp?
2. Define slew rate and what happens if it is very less?
3. What are the functions of pin 1 &5 in op amp IC 741?
4. What are the different applications of integrator and differentiator?
5. What are the advantages of practical integrator & differentiator compared with their ideal circuits?

Experiment no:8

PHASE LOCKED LOOP

AIM: To design PLL Circuit for required Oscillating, Capture & lock Frequencies

EQUIPMENTS & COMPONENTS: 1. PLL Trainer board
2. Dual trace oscilloscope
3. Digital frequency counters
4. Digital multimeter

THEORY: A PLL is basically a closed loop feedback system. The basic purpose of the PLL is to synchronize the frequency of the voltage controlled oscillator with that of the incoming signal ,It goes through the following three stages

Free running: When the control voltage given as input to the VCO Is zero, then VCO is said to be in free running mode

Capture: When the control voltage is applied as input to VCO, which forces the VCO to change its output frequency to move towards the frequency of the incoming signal until the two frequencies become equal is called capturing

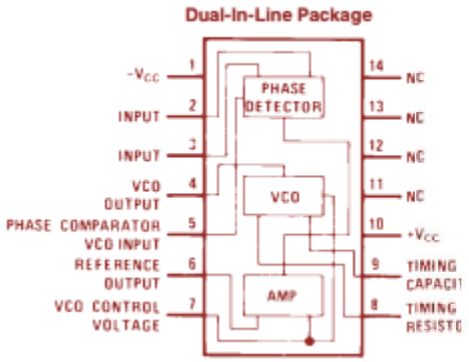
Locked: when two frequencies (Input & Output) are equal ,then circuit is said to be locked .The total time taken by PLL to establish lock is called as pull in time

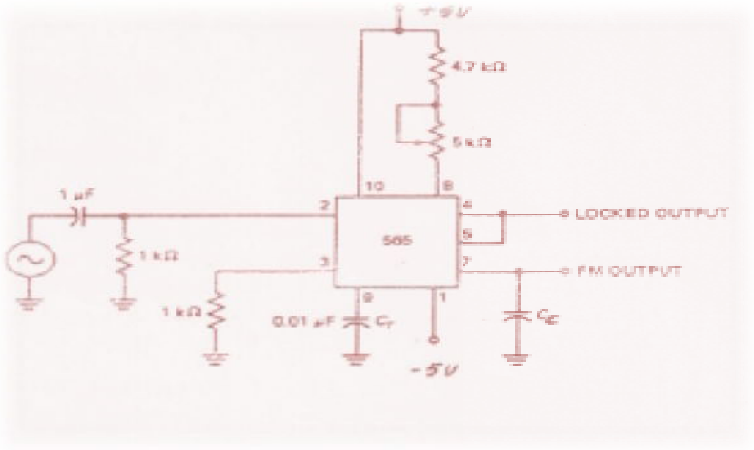
Free Running Frequency, $F_O = \frac{0.3}{Rt\ Ct}$, $C_t = 0.01\mu F$, $R_t = 6\ K\Omega$

Capture Frequency, $F_C = \frac{1}{2\pi}\sqrt{\frac{2\pi FL}{RfCf}}$

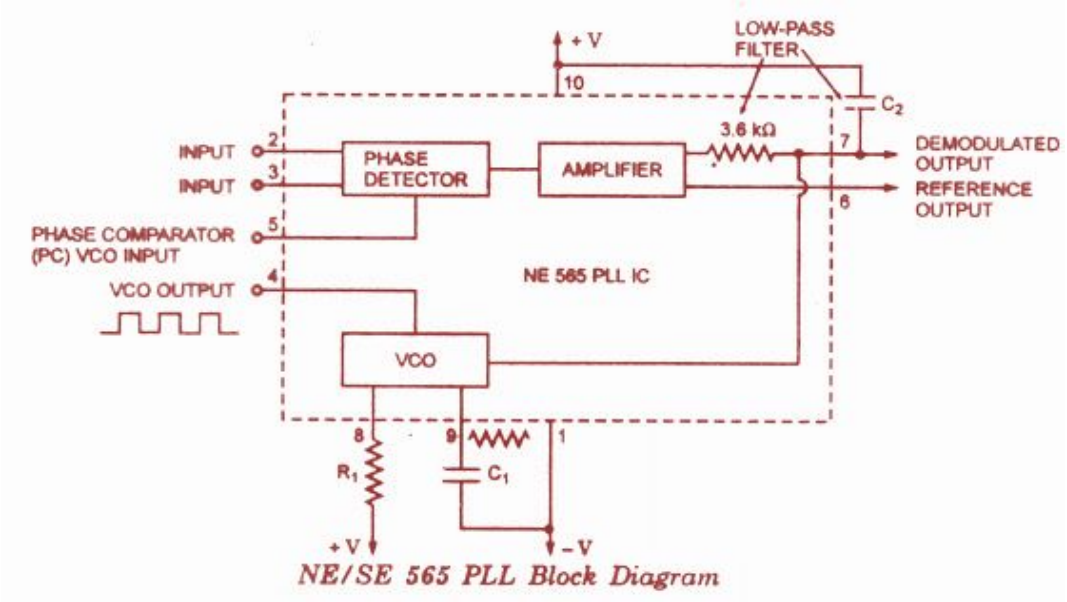
Locked Frequency, $F_L = \pm\frac{8Fo}{Vcc}$,$V_{CC} = +V_{CC} - (-V_{CC})$

PLL IC 565 PIN & CIRCUIT DIAGARM





PLL BLOCK DIAGRAM



NE/SE 565 PLL Block Diagram

PROCEDURE:

Free running Frequency:

1.Switch on the trainer and measure the output of the regulated power supplies i.e. +12V and ± 5V. These supplies are internally connected to the circuit, so no extra connections are required.

2. Adjust the input to 1 V pp of 5 Khz frequency. and connect as input between pin 2 & 3

3.Calculate the free-running frequency range of the circuit for different values of timing resistor R_t (to measure the R_t—Switch off the trainer and measure the R_t value using digital multimeter between two given test points) and record the frequency values in table1

4. Connect 0.1μf capacitor (C_C) to the circuit and open the loop by short between pin 4 and pin5. Measure the minimum and maximum free-running frequencies obtainable at the output of the PLL (pin4) by varying the pot. Compare your results with your calculations from step 3 (theoretical value). Simultaneously you can observe the output signal using CRO.

Lock Range:

5. Calculate the lock range of the circuit for a 5 kHz free-running frequency and record in table 2.

6. Connect pin 4, 5 with the help of springs and adjust potentiometer to get a free-running frequency of 5 kHz. Connect square wave generator output to the input of the PLL circuit. Provide a 5 kHz square signal of $1V_{pp}$ approximately (make this input frequency as close to the VCO frequency as possible).

7. Connect the frequency counters or CRO both channels to the input and output of the PLL.

8. Observe input and output frequencies while slowly increasing the frequency of square wave at the input. For some range output and input are equal this known as locking and PLL said to be lock with the input signal. Record the frequency at which the PLL breaks lock (output frequency of the PLL will be around VCO frequency and in oscilloscope you will see a jittery waveform when it breaks lock instead of clean square wave). This frequency is called the upper end of lock range and records this as F2.

9.Beginning at 5khz slowly decrease the frequency of the input and determine the frequency at which the PLL breaks lock on the low end and record it as F1.

10. Find lock range from F2-F1 and compare with the theoretical values from step5.

Note:-C_2 (Filter capacitor) is used to eliminate possible oscillation in the VCO voltage

Capture range:

11.Calculate the capture range of the circuit for a 5 kHz free-running frequency (consider filter capacitor C_c) is 0.1μf.

12.With the oscilloscope and counter still on pin4, slowly increase the input frequency from minimum (say 1 kHz). Record frequency (as F3) at which the input and output frequencies of the PLL equal, this is known as lower end of the capture range.

13.Now keep input frequency at maximum possible (say 10 kHz) and slowly reduce and record known as upper end of the capture range.

14.Find capture range from F4-F3 and compare it with the theoretical value (from step 10).

15.Repeat the step from 10 to 13 C_c value 0.2µf.

Table 1 Free-running Frequency (F o)

C_t =0.01µF

S.no	**R_t (Pot) value**	**Theoretical frequency(F_0) KHz**	**Practical frequency(F_0) KHz**
1.	5KΩ		
2.	6KΩ		

Table 2 for Lock range(F L)

S.no	**R_t (Pot) value**	**Theoretical frequency(F_L) KHz**		**Practical frequency(F_L) KHz**	
		F_1	F_2	F_1	F_2
1.	5KΩ				
2.	6KΩ				

Table 3 for Capture range **(F_C)**

Filter Capacitor C_f = 0.1µF

S.no	**R_t (Pot) Value**	**Theoretical frequency(F_C) KHz**		**Practical frequency(F_C) KHz**	
		F_3	F_4	F_3	F_4
1.	5KΩ				
2.	6KΩ				

SAMPLE CALCULATIONS:

i) Free-running Frequency $F_O = \frac{0.3}{Rt\ Ct}$, for C_t = 0.01µF, R_t=5 KΩ

= 6Khz

ii) Locked Frequency, $\Delta F_L = \pm \frac{8Fo}{Vcc}$,$V_{CC} = +V_{CC} - (-V_{CC})$

$= +5-(-5) = 10v$

$= \pm \frac{8 \times 6 \times K}{10} = \pm 4.8$ Khz

$F_1 = F_O + \Delta F_L$ $F_2 = F_O - \Delta F_L$

$= 6+4.8$ $= 6-4.8$

$= 10.8$ kHz $= 1.2$ kHz

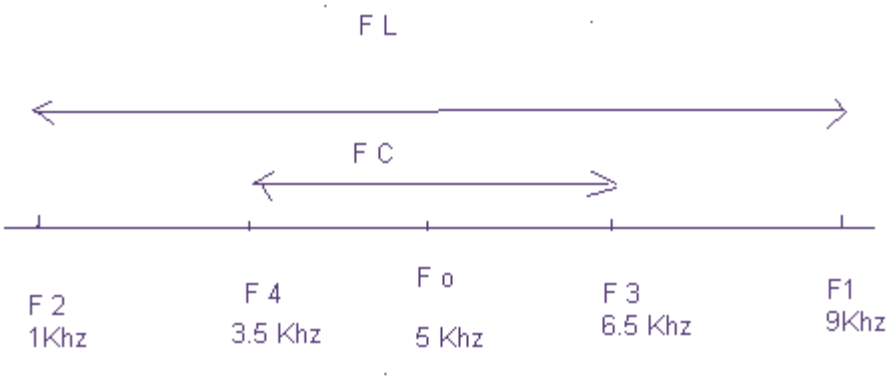
iii) Capture Frequency, $\Delta F_C = \pm \frac{1}{2\pi}\sqrt{\frac{2\pi FL}{RfCf}}$

where $Rf = 3.6k\Omega, Cf = 0.1\mu F$

$\Delta F_C = \pm 1.45$Khz

Note : F L > F c

NATURE OF GRAPH:



DICUSSION ON RESULT: Students will be able to observe
1.That oscillating frequency of PLL decides the capture & lock frequencies
2.Response of filter is varied if capacitor Cf & Rf is changed

PRELAB QUESTIONS:

1.Define lock range ,capture range & free running frequency for PLL
2.What are the applications of PLL?
3.What is VCO what is its output ?
4.What is the function of phase detector

Experiment no:9

SYNCHRONOUS COUNTERS

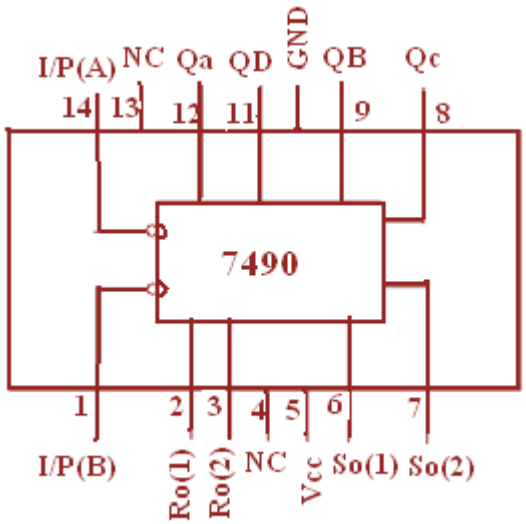
AIM: 1. To design and study a synchronous counter using 7490 I.C
2. Design a Mod 10 & Mod 6 counter

EQUIPMENTS & COMPONENTS: 1.Digital IC Trainer Kit
2.Multimeter
3.Connecting patch chords.
4.+ 5V Power supply
5. IC 7490
6.7408 AND Gate IC
7.Single Stand Wires

THEORY:7490 consists of four flip-flops internally connected to provide a mod 2 counter and a mod 8 counter can be used independently or in combination. Flip-flop A operates as a mod 2 counter where as the combination of flip-flop B, flip-flop C, Flip-flop D form a mod 8 counter.

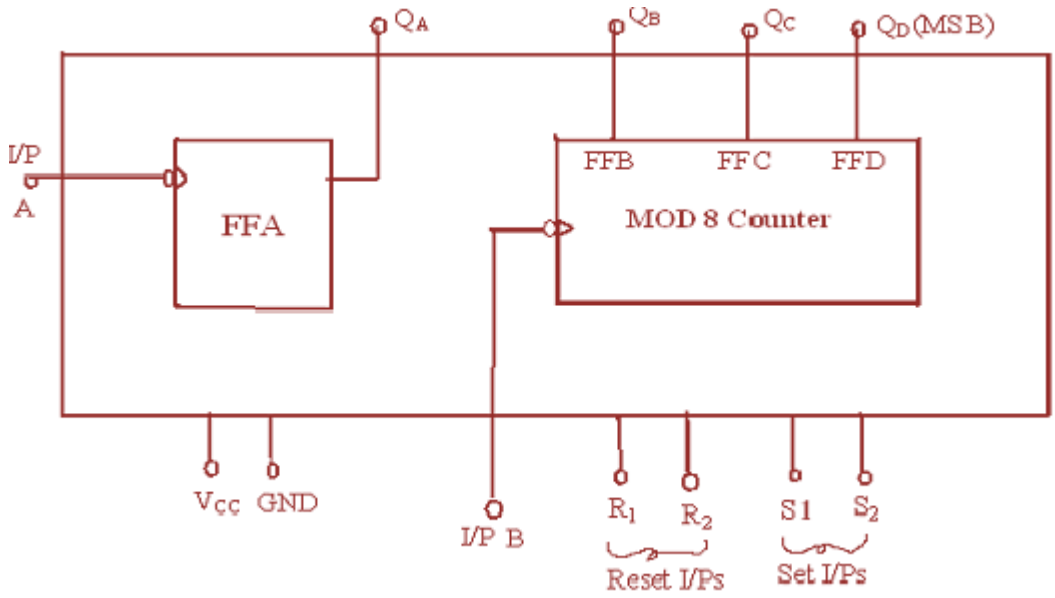
There are two reset inputs R_1 and R_2 both of which are to be connected to logic 1 for clearing all the flip-flops.The two set inputs S_1 and S_2 when connected to logic 1 are used for setting the counter to 1001.

PIN DIAGRAM 7490 :



NC → No connection
$R_{0(1)}, R_{0(2)}$ → Reset pins
$S_{0(1)}$, $S_{0(2)}$ → Set pins
I/P(A), I/P(B) → Clock I/Ps
V_{cc} → pin 5
GND → pin 10

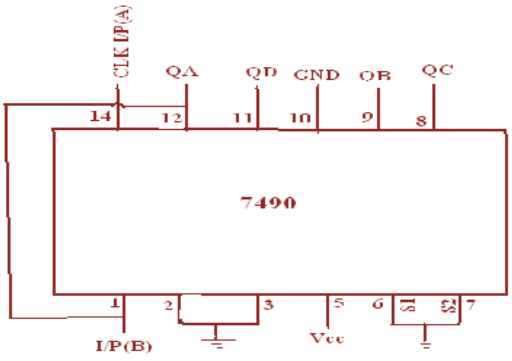
CIRCUIT DIAGRAM:

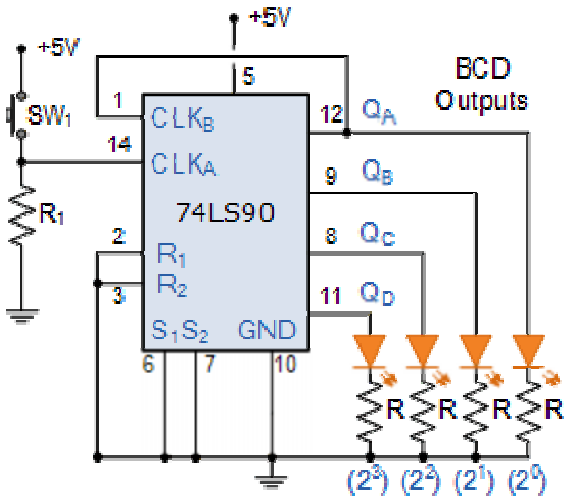


PROCEDURE:

1. Connect the circuit of 7490 for BCD count as shown in the circuit.
2. Observe the full count of mod 10.
3. Using AND gate design a mod-6 and mod-5 counter.
4. Short Reset pin to the output of AND gate.
5. Verify corresponding MOD count

MOD – 10

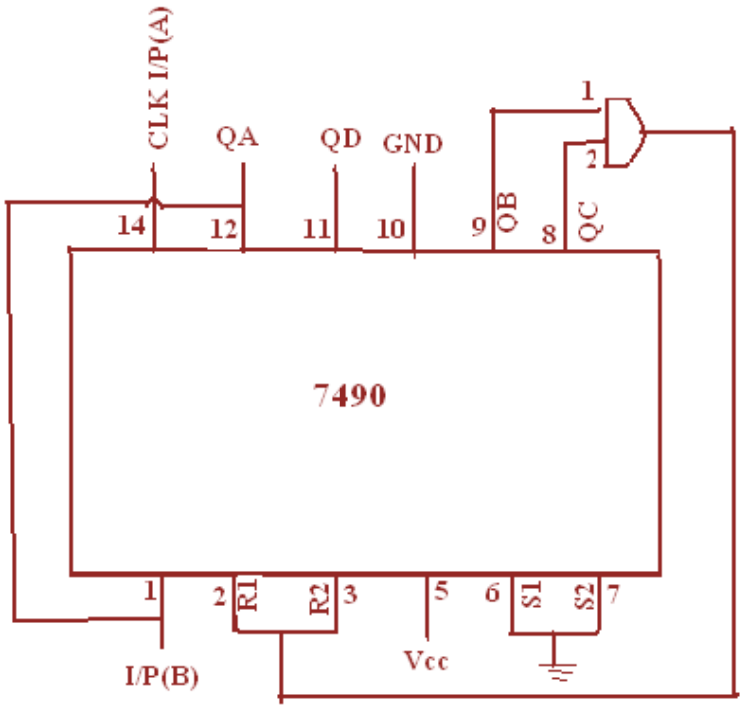




Truth Table

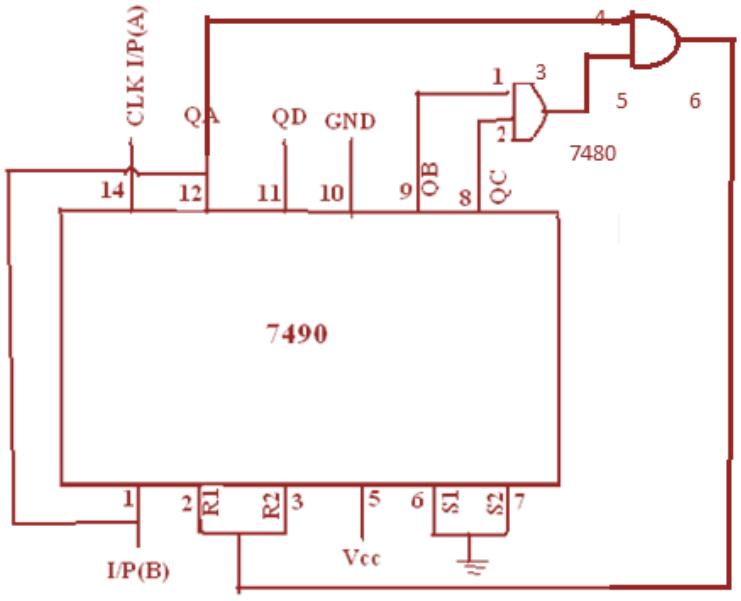
	count	Q_D	Q_C	Q_B	Q_A
0	[start]	0	0	0	0
	1	0	0	0	1
	2	0	0	1	0
	3	0	0	1	1
	4	0	1	0	0
	5	0	1	0	1
	6	0	1	1	0
	7	0	1	1	1
	8	1	0	0	0
	9	1	0	0	1
10	[new cycle]	0	0	0	0

Design mod-6 B.C.D Counter using I.C 7490



State	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	0	0	0

Design mod-7 B.C.D Counter using I.C 7490



Truth Table:MOD-7

State	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	0	0	0

DICUSSION ON RESULT: Students will observe

1. When AND gate is connected ,the count of synchronous counter resets
2. Synchronous counter of any mod value can be implemented using reset pins connected to respective output terminals

PRELAB QUESTIONS: 1.Define synchronous counter
2. What is a ripple counter?
3. Why do we use AND gate to reset?

Experiment no:10

ASYNCHRONOUS COUNTERS

AIM: 1. To design and study a 4 bit Asynchronous counter using flip flop I.C
2. Design Mod 12 asynchronous counter using 7473 flip-flops

EQUIPMENTS & COMPONENTS:
1. Digital IC Trainer kit
2. Multimeter
3. Connecting patch chords.
4. + 5V Power supply
5. IC 7473 (2 nos)
6.7400 NAND Gate IC
7. Single Stand Wires

THEORY: Give the maximum count the number of flip-flops required will be $N=2^n$ Here the output of previous flip flop acts as clock input to the next flip Flop. Thus increasing the propagation time. Nand gate is used to reset count

Procedure:

1.Connect all flip-flops as a ripple counter as shown in figure (1)

2.Find the binary number for last state is reset state.

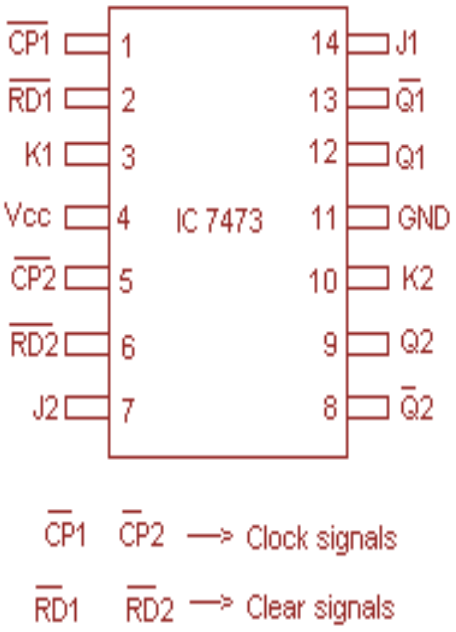
3.Connect all the flip-flops outputs that are 1 at the last state as the inputs to the NAND gates.

4. Connect the NAND gate output to the clear input of all flip-flops.

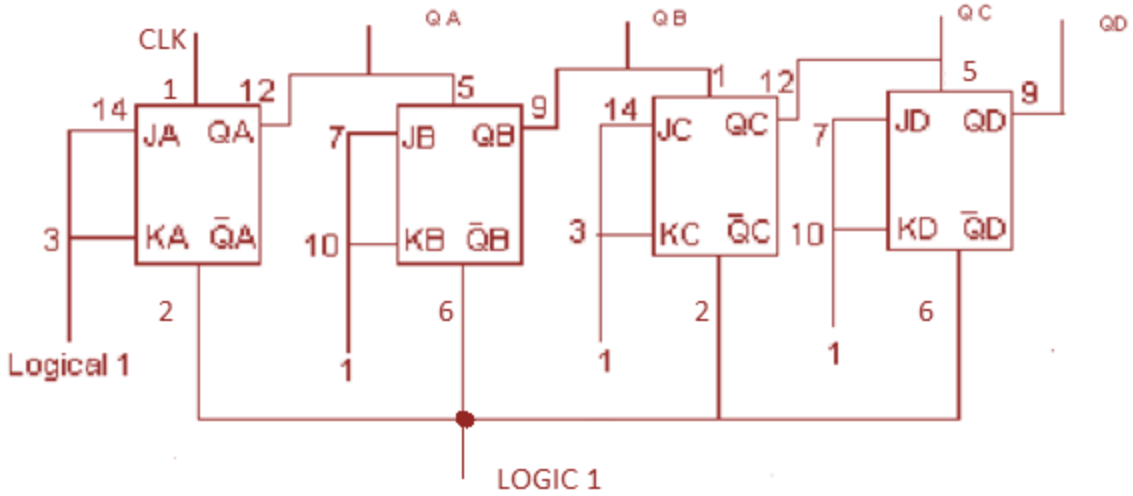
5. Switch Power ON and verify that it reads 0 to 15 [0000 to 1111] after 1111 it again resets 0000.

6. Later for fig (2) connections it reads 0 to 11 [0000 to 1011] after 1011 it again resets 0000. Therefore cycle of 0000 to 1011 repeats.

PIN DIAGRAM:



4 Bit Asynchronous counter(MOD 16 - 7473 2 ICs)

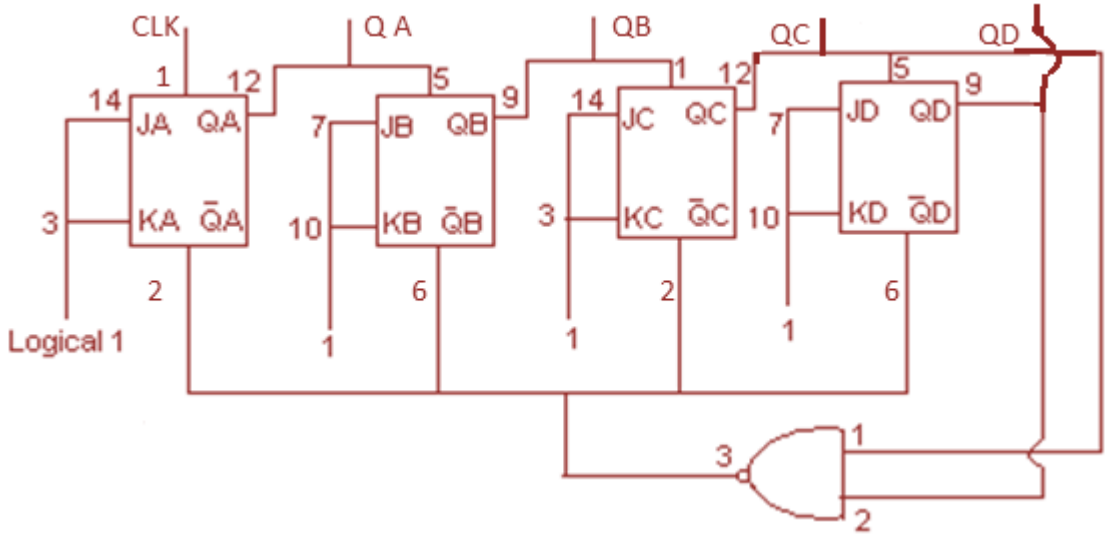


Implementation of Mod 16 Asynchronous counter

Truth Table:MOD 16 Counter

State	Qd	Qc	Qb	Qa
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
New cycle	0	0	0	0

Implementation of Mod 12 Asynchronous counter



Truth Table:MOD 12 Counter

State	Qd	Qc	Qb	Qa
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
New cycle	0	0	0	0

DISCUSSION ON RESULT: Students will observe

1. When NAND gate is connected the count of asynchronous counter resets
2. Asynchronous counter of any mod value can be implemented using reset pins connected to respective output terminals using flip flops

PRELAB QUESTIONS:

1. What is a decade counter?
2. Compare asynchronous and synchronous counters
3. Define propagation delay.
4. Mention Differences between a flip flop and latch

Experiment no:11

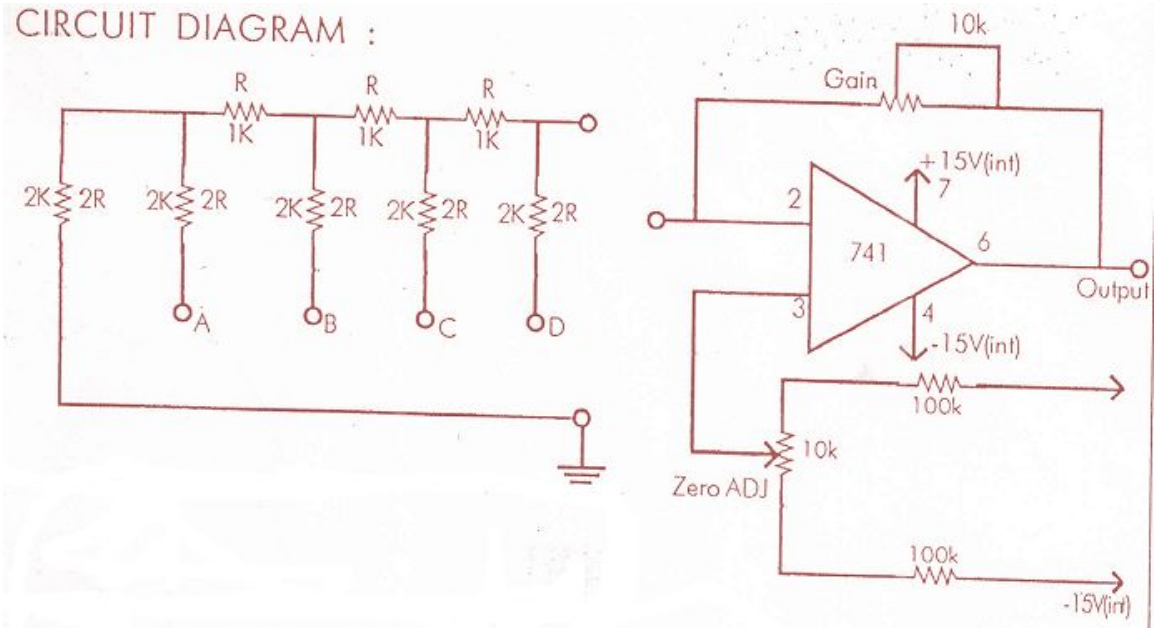
D/A CONVERTER- R-2R LADDER

AIM: To study and obtain the practical analog output for a 4-bit R-2R ladder type DAC using op-amp.

EQUIPMENTS & COMPONENTS: 1. Op-amp IC 741
2. Resistors 1KΩ,2KΩ
3. Dual Power Supply ±15V
4. Multimeter
5. CRO
6. Connecting wires

THEORY:-In R-2R ladder type D to A converter, only two values of resistors is used (i.e. R and 2R). The typical values of R are from 2.5KΩ to 10KΩ. In this output voltage is a weighted sum of digital inputs. Since the resistive ladder is a linear network, the principle of super position can be used to find the total analog output voltage for a particular digital input by adding the output voltages caused by the individual digital inputs.

Circuit Diagram:-



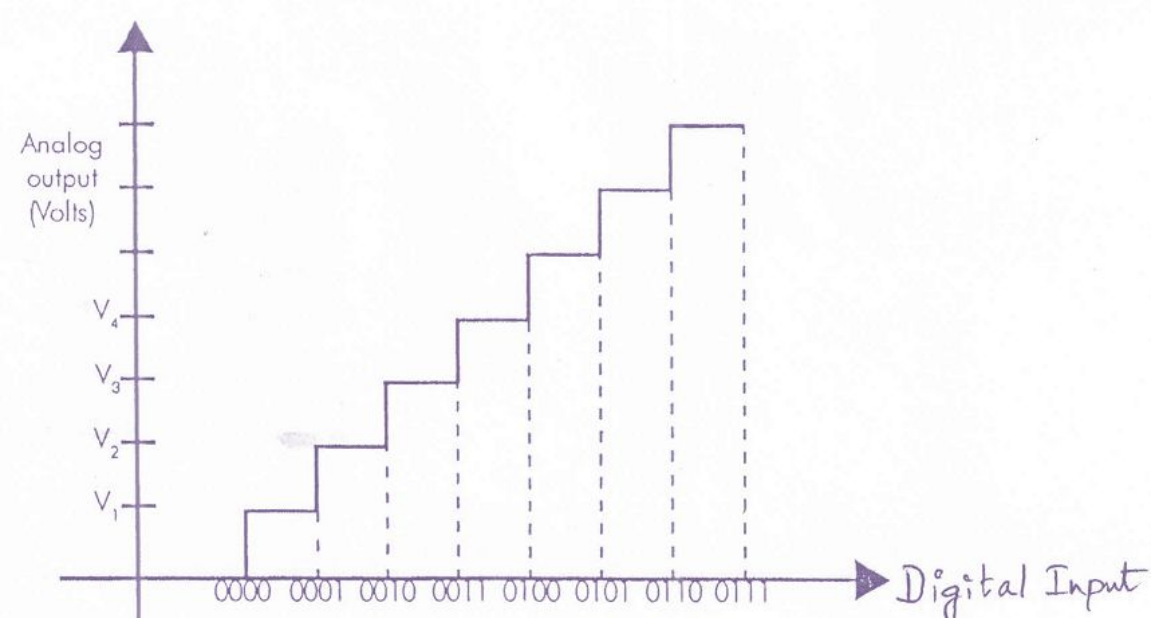
PROCEDURE:

1. Switch on the D/A Trainer kit.
2. Connect the four logical inputs provided on the kit to A, B, C, D terminals.
3. Connect the ladder network output to the input of the summing amplifier.
4. Connect the multimeter to the output of summing amplifier.
5. Set the offset voltage to zero by using zero adjustment pot with zero input (between pin 2 and GND).
6. By keeping input at logic 1 (LSB 0001) adjust the gain to some constant voltage. For example 0.25V or 0.5V.
7. By varying the logical inputs observe the output increasing according to the input.
8. Apply the clock to the input of decade counter and observe the output on CRO.
   (Connect ABCD of R-2R ladder network to counter Q_A, Q_B, Q_C & $Q_{D)}$
9. Observe the Stair case waveform on CRO and calculate the resolution.
10. Draw the graph between Analog equivalent of digital input Vs Analog output and observe the linearity.

TABULAR COLUMN:

S.No	Digital Input				Analog Output (Theoritical) (in Volts)	Analog equivalent of Digital input (in Volts) 'Δ'	Analog Output (in Volts) 'E'
	D	C	B	A			
1	0	0	0	0			
2	0	0	0	1			
3	0	0	1	0			
4	0	0	1	1			
5	0	1	0	0			
6	0	1	0	1			
7	0	1	1	0			
8	0	1	1	1			
9	1	0	0	0			
10	1	0	0	1			
11	1	0	1	0			
12	1	0	1	1			
13	1	1	0	0			
14	1	1	0	1			
15	1	1	1	0			
16	1	1	1	1			

EXPECTED WAVEFORM:



Calculations:

(1) $V_o = -V_R \frac{R_f}{R}\left[\frac{b_1}{2^1}+\frac{b_2}{2^2}+\frac{b_3}{2^3}+\frac{b_4}{2^4}\right]$

Where Reference Voltage, V_R=5V (given)

b_1 = D, b_2 = C, b_3 = B & b_4 = A

(2) Resolution, **Res = 1/ (2^n-1)**
Where 'n' is no. of bits.

(3) Linearity Error (LE): It is the difference between expected output and actual output.

% LE = (E-Δ) x 100

DISCUSSION OF RESULT:- Students will observe and discuss
1.Linearity and resolution of DAC
2.Output response step wise for various digital inputs changes for change in resolution

PRELAB QUESTIONS:

1. Mention any two specifications of a DAC.
2. Name any two types of DAC.
3. Advantages & Disadvantages of R-2R ladder DAC over Binary weighted DAC
4. Define resolution, monotonicity and accuracy with respect to DAC.
5. What is the range value for resistor (R) in DAC?

Experiment no:12

A/D CONVERTER

AIM: To study the operation of an 8 bit SAR type ADC and compare the theoretical and practical digital outputs.

EQUIPMENTS & COMPONENTS: 1. ADC 0808 IC
2. Connecting wires
3. Digital Multimeter
4. Trainer kit

THEORY:

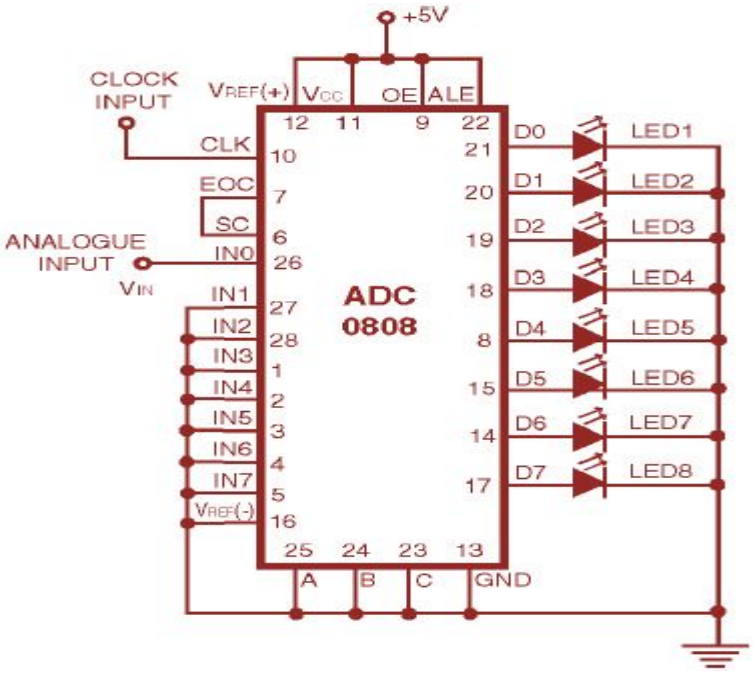
Analog to Digital converters are used in all computer applications that require interface with the analog world. In addition, if a digital read out of an analog measurement is needed, a stand-alone ADC can be used to generate the bit patterns required to drive a decimal or hexadecimal display. The **ADC0808** ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit Analog-to-digital converter, 8-channel multiplexer and Microprocessor compatible control Logic The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized Comparator a 256R voltage divider with Analog Switch tree and a successive approximation Register The 8-channel multiplexer can directly access any of 8-single-ended Analog signals.

PROCEDURE:

1.Connect clock pulse to the clock input of IC ADC 0808 to apply analog signal.
2.Connect multimeter across analog signal .
3.Switch power supply
4.Now increase the analog input voltage using knob in steps of 0.5V.
5.Measure the two voltages V_a and V_R using digital multimeter.
6.Verify the digital output by observing LEDs & tabulate them
7.Compare theoretical and practical values.

PIN DIAGRAM OF 0808 ADC

CIRCUIT DIAGRAM:



TABULAR COLUMN:

S. no	I/p V	O/p V	Digital output Theoretical								Digital output display							
1	0		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
2	0.5																	
3	1																	
4	1.5																	
5	2																	
6	2.5																	
7	3																	
8	3.5																	
9	4																	
10	4.5																	
11	5																	

DISCUSSION ON RESULT: Students will observe

1.Successive approximation register A to D Converter specifications practically

2.Change in digital output for various analog input ranges .

PRELAB QUESTIONS:

1. What are the different specifications of a ADC ?.
2. Name different types of ADC.
3. What are the Advantages & Disadvantages of SAR Type ADC over Dual Slope type ADC?.
4. What are the Advantages of DAC over ADC ?.

Experiment no:13

MONOSTABLE MULTIVIBRATOR USING IC 555

AIM: To study the operation of a Monostable multivibrator using 555 IC

EQUIPMENTS & COMPONENTS:

1.C.R.O
2.Function generator
3. Multimeter
4.Bread board
5. ± 15 V variable power supply
6. 555 Timer IC
7. Resistors 10k
8. Capacitors 0.1µF,0.01µF(2)
9.Single stand wires

THEORY: Monostable Multivibrators has one stable state and other is a quasi stable state. The circuit is useful for generating single output pulse at adjustable time duration in response to a triggering signal. The width of the output pulse depends only on external components, resistor and a capacitor.

The stable state is the output low and quasi stable state is the output high. In the stable state transistor Q1 is 'on' and capacitor C is shorted out to ground. However upon application of a negative trigger pulse to pin2, Q1 is turned 'off' which releases the short circuit across the external capacitor C and drives the output high. The capacitor C now starts charging up towards V_{cc} through R_A. However when the voltage across C equal 2/3 V_{cc} the upper comparator output switches form low to high which in turn drives the output to its low state via the output of the flip flop. At the same time the output of the flip flop turns Q1 'on' and hence C rapidly discharges through the transistor. The output remains low until a trigger is again applied. Then the cycle repeats.

The pulse width of the trigger input must be smaller than the expected pulse width of the output. The trigger pulse must be of negative going signal with amplitude larger than 1/3 Vcc. The width of the output pulse is given by,

$$T = 1.1\ R_A C$$

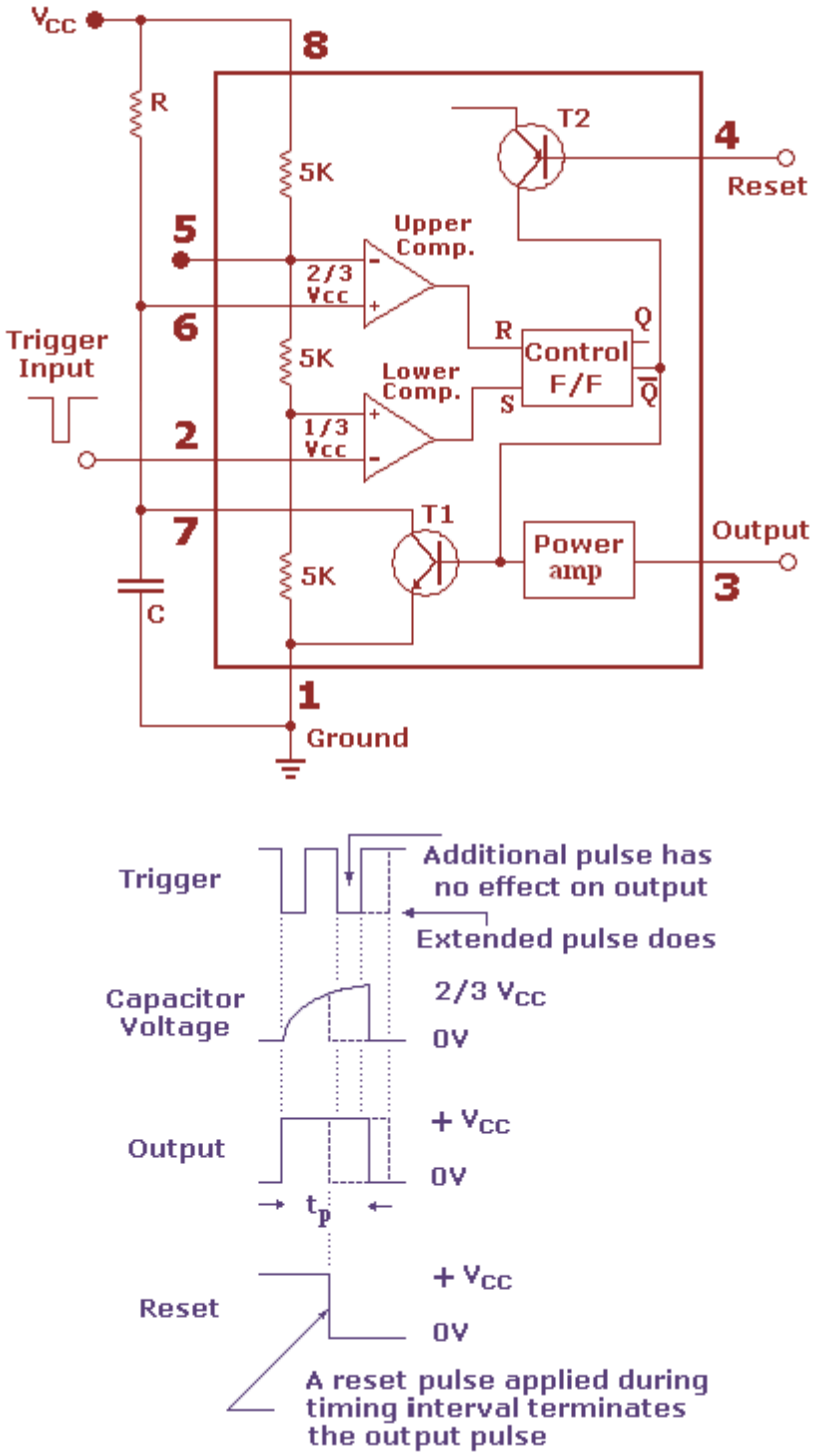


Figure 2: Waveforms for IC555 Monostable Multivibrator

Note:Once triggered, the circuits output will remain in the high state until the set time tp elapses. The output will not change its state even if an input trigger is applied again during this time interval tp.

DESIGN:

Given a pulse width of duration of 100 µs

Let C = 0.01 µF; Frequency = _____KHz

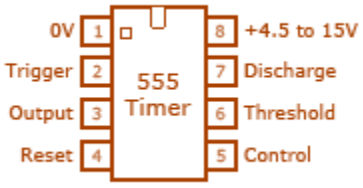
Here, T= 1.1 R_AC

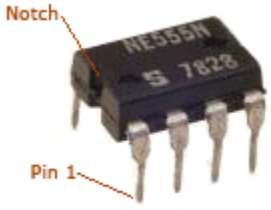
So,calculate R_A =

PROCEDURE:

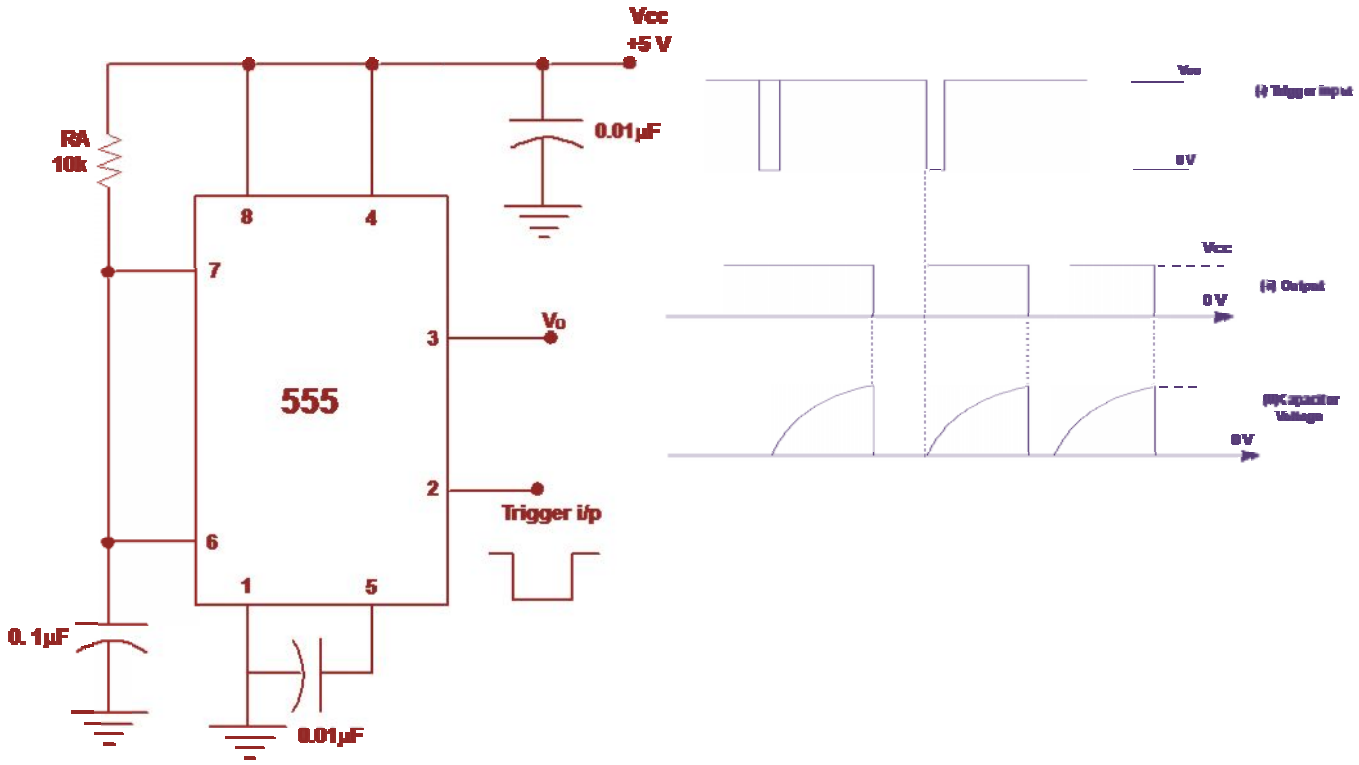
1. Rig-up the circuit of 555 monostable Multivibrators as shown in fig with the designed value of components.
2. Connect the trigger input to pin 2 of 555 timer form the function generator.
3. Connect the CRO probes to pin 3 and 2 to display the output signal and the voltage across the timing capacitor. Set suitable voltage sensitively and time-base on the CRO.
4. Switch on the power supply to CRO and the circuit.
5. Observe the waveforms on the CRO and draw to scale on a graph sheet. Measure the voltage levels at which the capacitor starts charging and discharging, output high and low timings along with trigger pulse.

555 IC Pin diagram:





CIRCUIT DIAGRAM 555 TIMER MONOSTABLE MULTIVIBRATOR WITH INPUT OUTPUT MODEL WAVEFORMS:



Sl.no	Trigger input pulse Voltage	Resistor	capacitor	output voltage	Theoretical Time period	Practical Time period
1.						
2.						
3.						
4.						

DISCUSSION ON RESULT:

Student will observe

1. Monostable Multivibrators output frequency changes as the voltage across capacitor is varied by selecting different value capacitors
2. Output amplitude changes when Vcc to 555 IC is varied between 5V to 18V
3. Once triggered, the circuits output will remain in the high state until the set time t_p elapses. The output will not change its state even if an input trigger is applied again during this time interval t_p.

PRELAB QUESTIONS:

1. What are the features of 555 timer?
2. What are the applications of 555 timer?
3. Define duty cycle ratio.
4. What are the applications of monostable Multivibrators?
5. What is meant by quasi stable state?
6. What should be the amplitude of trigger pulse?