A low power low ripple Schmitt trigger based PWM Boost Converter for Energy Harvesting Applications

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***Abstract*—The design of monolithic power management circuits is critical in energy harvesting applications. A Pulse width modulation (PWM) boost converter with feedforward and feedback control mitigates the changes in input-output parameters and avoids the use of compensation circuit. However, the conventional design of a clock generator in feedback path employs power hungry comparators and latches. This paper proposes an improved design of clock generator replacing comparators and latches with a schmitt trigger circuit. As a result, a low power and a low ripple PWM was acheived. The design was implemented in UMC 180 nm CMOS technology generating a stable output of 3.3 V for an input range of 1.2 V - 1.6 V. Due to the application of the proposed technique, a reduced power consumption of 60.19 mW and low ripple voltage of 18.29 mV was achieved, for a maximum load current of 100 mA at an efficiency of 98%. Thus making the design suitable for energy harvesting applications.**

***Index Terms*—Energy Harvesting, Power management, PWM Boost Converter, Schmitt Trigger**

I. Introduction

Energy harvesting is emerging as the key research area for low-power applications in battery driven devices used in medical equipments, consumer electronics, wearable electronics and military applications. The design of power management unit for energy harvesting applications is heavily dependent on the efficient design of the boost converter. Pulse width modulation (PWM) based boost converters have been widely implemented due to the simplicity and compactness of design [1]–[3]. These PWM based converters can be classified into voltage, current and hysteresis controlled converters. The converters based on current control technique are complicated and are difficult to stabilize. Whereas, the voltage controlled boost converters are relatively straight-forward but the output stability is dependent on the compensation circuit [2]. This compensation circuit is circumvented by using a feedforward and feedback loop control thus making the circuit more agile. Using this compensation free technique, a boost converter was designed employing a ramp based clock generator consisting of two hysteresis comparators and one SR latch [3]. Yet, this circuit gives a ripple of 36.52 mV with 93% efficiency and power dissipation of 348 mW. Even though this work is able to eliminate the compensation circuit, it has a power consumption of the order of hundreds of milli watts and is also area hungry.

The problem of area and power can be resolved by using a schmitt trigger for designing ramp based clock generator [4]. In this paper, it is proposed to use the aforementioned ramp based clock generator to design a PWM based boost converter which consumes low power and low area. The effective power consumption is reduced to the order of 10's of milliwatts, with good line and load regulation. The proposed boost converter is designed for an input voltage range of 1.2 V - 1.6 V generating a stable output voltage of 3.3 V with a load current of 100 mA. Design aspects that are commonly used is the provision of the back gate diode which is connected across the switching transistor [5]. Ripple voltage and efficiency are also key factors governing the design of a low power DC-DC converter [6]. Any changes in the input voltage results in a corresponding change in the output voltage which is balanced by the feedback mechanism to bring stability to the output. The generation of a ramp signal from a fixed duty cycle clock pulse was described in [7] and has been further enhanced in [8] and the same is applied in the proposed design. These specifications are suitable for the design of an energy harvesting circuit aimed at driving a wireless sensor node [9].The detailed circuit description of feedforward and feedback circuit along with the proposed design of boost converter using ramp based clock generator with Schmitt trigger circuit is elucidated in section II. The design results are discussed in section III and conclusion is presented in section IV.

II. Circuit Description of Feedforward and Feedback Control of Boost Converter

The circuit consists of Ramp based Clock Generator, Hysteresis Comparator, Level Shifter and Non Overlapping Clock Buffer as per the schematic shown in Figure 1. It depicts the circuit design of the boost converter with feedforward and feedback control circuitry. The forward path consist of the power stage having inductor (L), MOS switches (MN0 & MP0) and load capacitance (C_L). The voltage divider circuit at the input stage consisting of R_{FF1} and R_{FF2} are used to generate voltage V_H given to the non inverting terminal of hysteresis comparator forming the feedforward path. The output of hysteresis comparator is given to a level shifter

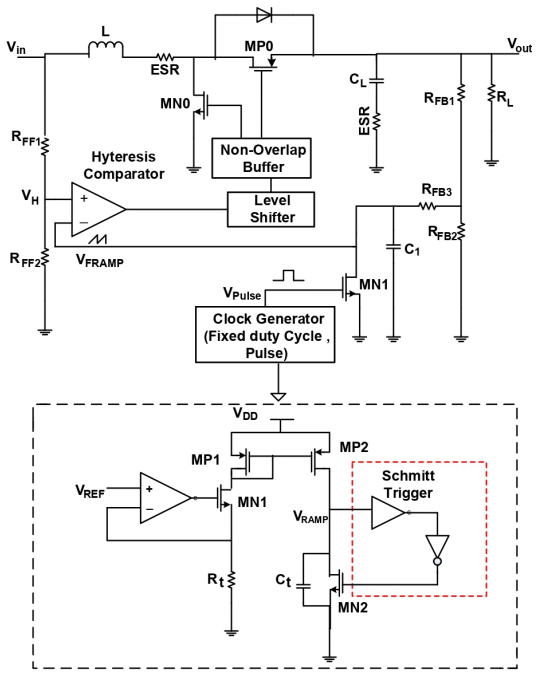

Fig. 1. PWM based Boost Converter

that is connected to a non-overlapping buffer which finally generates the pulse signals that control the switching action of MP0 and MN0. The voltage divider R_{FB1} and R_{FB2} samples the output voltage and is given to the capacitor (C_1) through R_{FB3}. The crucial component in this design is the transistor MN1 which is responsible for charging and discharging of the capacitor (C_1) to generate a ramp signal. This ramp signal is given to the inverting terminal of hysteresis comparator to complete the feedback loop. The frequency of the ramp signal is controlled by the clock generator.

The Clock generator consists of a PMOS current mirror using MP1 and MP2. The MN1 transistor is connected through a two stage operational amplifier connected in the active cascode mode to increase gain of the transistor. The transistor MN2 controls the switching action of capacitor (C_t), thus generating the ramp signal. The frequency of this ramp signal can be adjusted by the schmitt trigger and inverter, depicted in the red box, connected in the feedback loop to the gate of the transistor MN2.

The detailed schematic of clock generator predominantly consists of a Schmitt trigger circuit as shown in Figure 2, which converts the ramp signal into a pulse signal. The frequency of the generator can be measured with reference to Upper Trigger Point (UTP) and Lower Trigger Point (LTP) of Schmitt trigger circuit. It consists of three PMOS and three NMOS transistors. The two PMOS transistors (M_{U1} and M_{U2}) and two NMOS transistors (M_{L1} and M_{L2}) are fed with a ramp input [10]. As the ramp voltage is rising from 0V, the bottom two transistors (M_{L1} and M_{L2}) are off and output is at high level. When the ramp voltage rises to a value greater than the voltage required to turn bottom transistor ON, the output switches to low voltage at this UTP. Similarly the LTP can be obtained in the reverse direction. The transistor aspect ratio(W/L) can be varied to control the UTP and LTP and the same is governed by equation (1) and (2),

$$\frac{K_{L1}}{K_{L3}} = \left\{ \frac{V_{DD} - V_{UTP}}{V_{UTP} - V_{TN}} \right\}^2 \tag{1}$$

$$\frac{K_{U1}}{K_{U2}} = \left\{ \frac{V_{LTP}}{V_{DD} - V_{LTP} - |V_{TP}|} \right\}^2 \tag{2}$$

The frequency of operation which is based on resistor (R_t), capacitor (C_t) and reference voltage (V_{REF}) of the ramp based clock generator is given in equation (3),

$$f = \frac{V_{REF}}{R_t C_t (V_{UTP} - V_{LTP})} \tag{3}$$

In this paper, this modified ramp based clock generator is used to implement the boost converter as shown in Figure 1. Thus automatically reducing the overhead of two hysteresis comparators and SR latch. Based on this contribution, this design achieves reduced power consumption of 60.19 mW when compared to the earlier value of 348 mW [3].

III. RESULTS AND DISCUSSIONS

The simulation results of the proposed boost converter is shown in Figure 3. The output stabilizes at a value of 3.37 V with a ripple of 18.29 mV after a transient time of 88 usec for an input voltage of 1.6 V.

The clock frequency of the circuit is 730 KHz with maximum output load current 100 mA and the ripple voltage is noted as 18.29 mV as shown in Figure 4. The duty cycle of the clock signal is based on both the feedforward and feedback components and any changes in the input and subsequent changes in the output will be balanced out by this mechanism to maintain a stable output voltage of 3.3 V.

The line regulation is performed at full load condition (I_L = 100 mA) with the input range of 1.2 V - 1.6 V and the output is depicted in Figure 5, which indicates a stabilized voltage of 3.3 V with line regulation of 235 mV/V. The input voltage is changed from 1.2 to 1.6 V at 0.4 msec and from 1.6 to 1.2 V at 0.75 msec.

The Figure 6 depicts stable performance of the boost converter for both light load (10 mA) and heavy load (100 mA) at an input voltage of 1.4 V, thus giving a load of regulation 10 mV/mA.

The power consumption of this circuit is 60.19 mW. It is observed that the duty cycle of the clock signal is 65%. Using the equation (4), and substituting the values of V_{out} to be 3.37 V and $V_{in(min)}$ to be 1.2 V, the efficiency of this circuit is calculated to be 98%.

$$Efficiency = \frac{V_{out}(1 - D)}{V_{in}} \tag{4}$$

It is evident from Table I that the variation of important design parameters with respect to corner conditions is marginal and the proposed design is stable at the process corners.

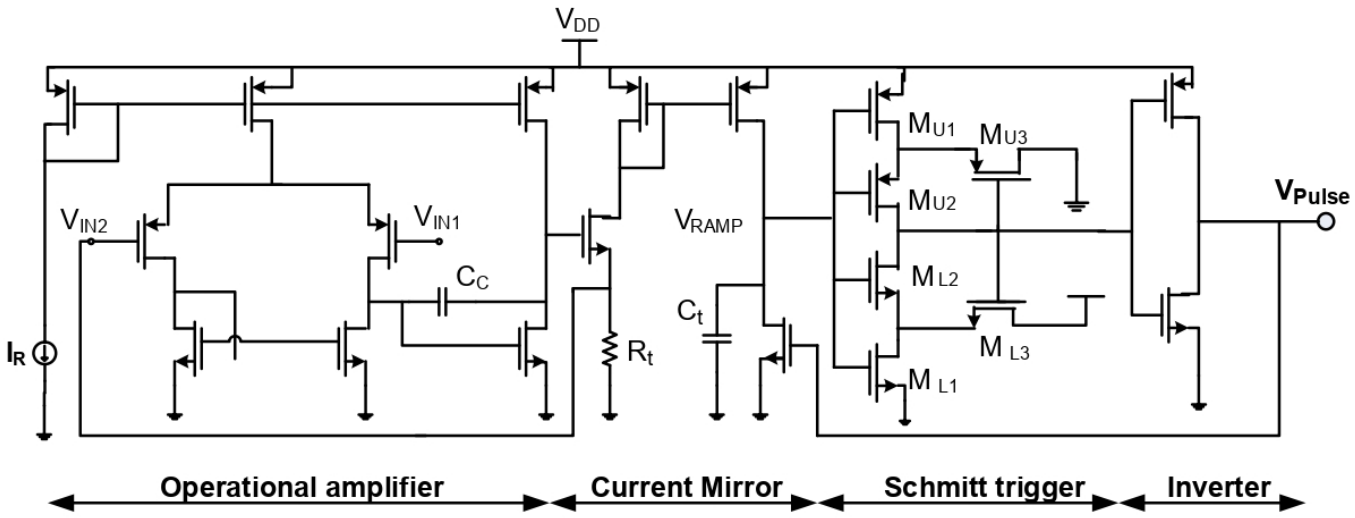

Fig. 2. Detailed schematic of proposed clock generator

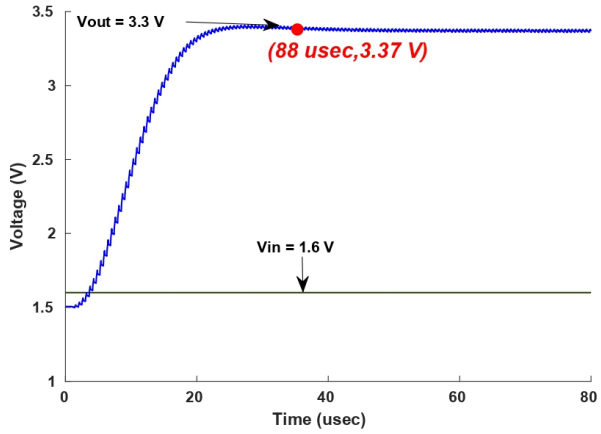

Fig. 3. Transient analysis of boost converter

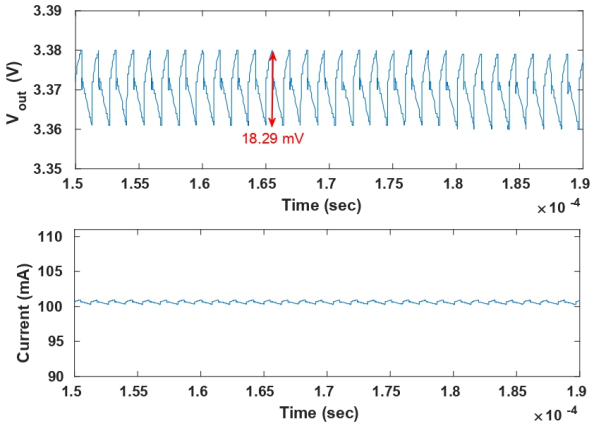

Fig. 4. Ripple voltage and load current

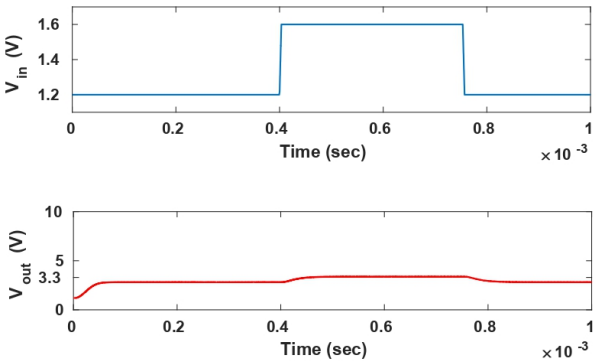

Fig. 5. Line Regulation.

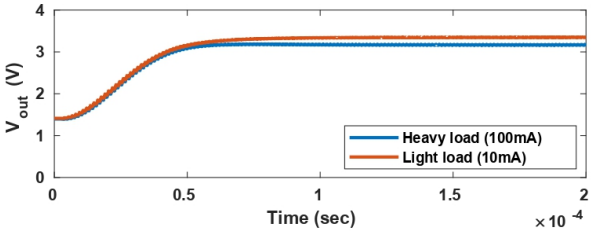

Fig. 6. Load Regulation.

TABLE I
SIMULATION RESULTS FOR CORNER CONDITIONS.

Parameter	FF	TT	SS
Input Voltage Range(V)	1.2-1.6	1.2-1.6	1.2-1.6
Iout (mA)	100	100	100
Output Voltage(V)	3.374	3.3714	3.361
Switching Frequency(KHz)	732	724	720
Ripple Voltage(mV)	19	18.29	17.43
Line Regulation(mV/V)	222	235	250
Load Regulation(mV/mA)	9.6	10	10.9
Power Efficiency	97.5	98	98.5

TABLE II
COMPARATIVE ANALYSIS WITH OTHER PUBLISHED PAPERS

Parameter	[3]	[5]	[6]	This work
Input Voltage Range(V)	1.2-1.6	0.8-3	3.3	1.2-1.6
Iout (mA)	100	0-150	14-110	100
Output Voltage(V)	3.3921	3.3	5.8-7	3.3714
Switching Frequency(KHz)	240	-	5500	724
Ripple Voltage(mV)	36.52	-	75	18.29
Line Regulation(mV/V)	237	100	-	235
Load Regulation(mV/mA)	5.48	100	-	10
Power Efficiency	93	95	77	98
Power Dissipation(mW)	348.19	-	300	60.19

Further, the results of the proposed work are compared with [3], [5] and [6] in Table II, it is established that the proposed method gives better performance in terms of reduction in power consumption from 348.19mW [3] to 60.19 mW. The other parameters like the ripple value of the proposed design is 18.29mV whereas in [3] it was 36.52 mV.

CONCLUSION

This paper establishes the design of a highly efficient boost converter generating an output voltage of 3.3 V at load current of 100 mA at a reduced power consumption of 60.19 mV and a low ripple voltage of 18.29 mV for an input range of 1.2 V - 1.6 V. Thus, concluding that the use of Schmitt trigger based ramp generator is more appropriate for designing a boost converter that can be utilized in energy harvesting circuits.

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