6.5.3 Quality assurance initiatives of the institution include:

1. Regular meeting of Internal Quality Assurance Cell (IQAC); Feedback collected, analysed and used for improvements
2. Collaborative quality intitiatives with other institution(s)
3. Participation in NIRF
4 .any other quality audit recognized by state, national or international agencies (ISO Certification, NBA)

Year	Confernces, Seminars, Workshops on quality conducted	Academic Administrative Audit (AAA) and initiation of follow up action	Participation in NIRF along with Status.	ISO Certification. and nature and validity period	NBA or any other certification received with program specifications.	Collaborative quality initiatives with other institution(s) (Provide name of the institution and activity)	Orientation programme on quality issues for teachers and students organised by the institution, Date (From-To) (DD-MM-YYYY)
2020-21	-	-	Yes	-	-	-	-
2020-21	-	Yes	-	-	-	-	-
2020-21	-	IQAC Meetings	-	-	-	-	-
2020-21	-	-	-	-	-	Yes	-
2020-21	Yes	-	-	-	-	-	-
2020-21	-	-	-	-	-	Yes	

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2020-21	-	-	Yes	-	-	-	-
2020-21	-	Yes	-	-	-	-	-
2020-21	-	IQAC Meetings	-	-	-	-	-
2020-21	-	-	-	-	-	Yes	-
2020-21	Yes	-	-	-	-	-	-
2020-21	-	-	-	-	-	Yes	

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National Institutional Ranking Framework
Ministry of Education
Government of India

India Rankings 2021:Participated Institutes Engineering

Institution list in alphabetical order

Back

Show 100 entries

Search: Muff

Name	City	State
Muffakham Jah College Of Engineering And Technology	Hyderabad	Telangana

Showing 1 to 1 of 1 entries (filtered from 1,143 total entries)

Previous 1 Next

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MUFFAKHAM JAH
COLLEGE OF ENGINEERING & TECHNOLOGY

(Estd. by sultan-Ul-Uloom Education Society in 1980)
(Affiliated to Osmania University, Hyderabad)
Approved by the AICTE & Accreditated by NBA

Date: 08-10-2020

INTERNAL NOTICE

In order to address the issues related to academic performance pertaining to theory and lab, of Mechanical Engineering Department, the following committee is constituted for Academic, Administrative and Audit work:

Committee Members

1. Head, MED
2. Dr. Md Viquar Mohiuddin, Prof., MED
3. Dr. Ishrat Meera Mirzana, Prof., MED
4. Dr. Mohammad Sadak Ali Khan, Prof., MED
5. Dr. D. Srinivas Rao, Prof., MED
6. Dr. O Hema Latha, Assoc. Prof., MED
7. Dr. Syed Khader Basha, Asst. Prof., MED

The committee named as "Academic and Administrative Audit committee" and its primary responsibilities of the committee is to,

1. Head acts as a Chair for the committee.
2. Understanding the current system and assessing the strengths and shortcomings of the Departments and Administrative Units, as well as suggesting ways to enhance and overcome the flaws.
3. Identifying bottlenecks in existing administrative systems and recommending solutions
4. Academic reforms, administrative reforms, and examination reforms.
5. Determine the most efficient use of money and other resources.
6. To offer techniques for continual quality improvement while keeping criteria and standards in mind.
7. Creating efficient teaching and learning methods
8. Course and Program Outcomes Evaluation
9. Creating a system for assessing students
10. Using co-curricular and extracurricular activities to ensure high-quality education.

30/09/2020

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Head, MED

HEAD
Mechanical Engineering Department
Muffakham Jah College of Engineering & Technolo
Road No:3, Banjara Hills,
HYDERABAD-500 034. T. S.

8-2-249 to 267, "Mount Pleasant" Road No.3, Banjara Hills, Hyderabad – 500 155
Phone: 040-23350523, 23352084, Fax: 040-2335 3428
Website: www.mjcollege.ac.in, E-mail: principal@mjcollege.ac.in

6-5-3 CIVIL

MUFFAKHAM JAH
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DEPARTMENT OF CIVIL ENGINEERING

Is organizing

A Webinar on
Sustainable Technologies for Waste Water Engineering - Case Studies of STPs
5th June 2021 from 11:00 AM to 12:30 PM

RELEVANCE OF THE THEME

Waste water treatment has assumed enormous importance in the light of the recently promulgated statutory regulations by National Green Tribunal for quality of effluent from STPs. Apart from lowering the limits on BOD, COD, TSS, the new regulations have specified the limits on Nitrogen and Phosphorous which were hitherto not stipulated. Not only the new STPs, but even the existing STPs are required to meet the new norms by undergoing upgradation process. The GoI has launched Jal Jeevan Mission (Urban) and SBM 2.0 Urban in 2021. While the AMRUT cities can draw funds for construction of STPs under JJM, all the statutory town are eligible to get funds for sanitation and STP projects under SBM 2.0 Urban. It is expected that in the coming years the Civil Engineers will be called upon to not only execute these projects but also be actively involved in their operation.

Speaker

Dr. D N Ravi Shankar

Ph D (Env Engg.)

- Served Bangalore Water Supply and Sewerage Board for 30 Years. Instrumental in setting up STPs for Bangalore city each of them sized up to 100's of MLD capacity.
- Member of Expert Committee constituted by Government of Karnataka for identification of sources for sustainable water supply to Bangalore city. He has been Technical Advisor to concerned Ministry, Govt. of Karnataka.

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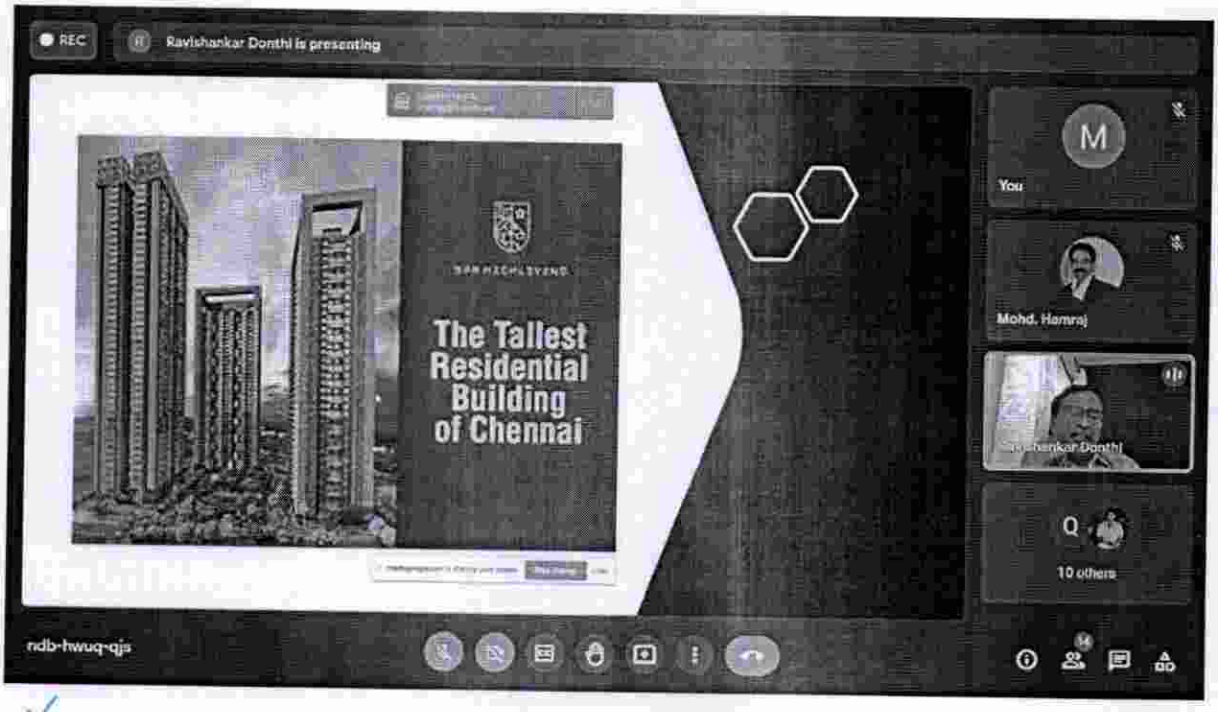
Head of Department, Civil Engineering introducing speaker



Dr. Ravi Shankar, speaker addressing the webinar

The webinar drew huge interest from the faculty, students, and industry experts not just from Hyderabad but from all over India, more than 500 participants joined the webinar and enriched their knowledge from the highly experienced speaker.

Youtube Link : https://www.youtube.com/watch?v=wv7QAm93DF8&t=183s

List of Participants of Webinar on "Sustainable Wastewater and Solid Waste Management - Case Studies" on 5th June 2021

Sl.No.	Name of the Participant (As required in the E-Certificate)	Faculty/ Student	Institute / University (As required in the E-Certificate)
1	Mohd Nazim Raza	Faculty	Muffakham Jah College of Enginnering and Technology
2	Dr.Mohd.Hamraj	Faculty	MJCET
3	SYEDA HUSNA NOOREEN	Faculty	Muffakhamjah college of engineering and technology
4	Asgar ullah khan	Faculty	Muffakham jah college of engineering and technology
5	Mr. Barkat Ali Khan	Faculty	Muffakham Jah college of Engineering & Technology
6	Syed Muzammil Shah	Faculty	Muffakham jah college of engineering and technology
7	Syed Saifuddin	Faculty	Muffakham Jah College of Engineering and Technology
8	Dr. Md. Abdullah Shariff	Faculty	MJCET
9	ABHIJEET DAS	Faculty	College Of Engineering and Technology
10	SABARINATHAN N	Student	SRM University
11	ANUSREE P	Student	VIMAL JYOTHI ENGINEERING COLLEGE CHEMPERI
12	B vinod naik	Student	Osmania university
13	A.Mahitha	Student	SRK Institute of Technology
14	S. C. Boobalan	Faculty	Sri Krishna College of Engineering and Technology
15	Mohammed Adil Ali	Student	Muffakhamjah college of engineering and technology
16	Mohammed Abdul Moyeed	Student	Muffakham Jah College of Engineering & Technology (MJCET) Laboratories & Workshops
17	PRUTHVIRAJ SR	Student	University BDT College of Engineering
18	K Sudheer	Student	Jaya Prakash Narayan College Of Engineering
19	Boga Divya	Faculty	Siddhartha institute of engineering &technology
20	Syed Shoaib Amaan	Student	Muffakham Jah College of Engineering and Technology
21	Ashveen Kumar Puppala	Faculty	Matrusri Engineering College, Hyderabad
22	Dr. Arunav Chakraborty	Faculty	Tezpur University
23	PUVIYARASAN.R	Student	BANNARI AMMAN INSTITUTION OF TECHNOLOGY
24	MD.Khasim Shareef	Student	ISL ENGINEERING COLLEGE
25	Arqam Azeem	Student	Muffakham Jah College of Engineering and Technology

Students of B.E ¾ -2nd Sem, CED,MJCET who got selected for Internship Programme-2019 along with Mr.Koundinya , Director, M/s Peketi Ventures Pvt. Ltd. and Prof.Mohd.Hamraj HOD (Civil),MJCET.

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List of Students for Internship in Peketi venture Private Limited

1	1604-16-732-003	MRS.NEHA TASLEEM	Peketi Ventures
2	1604-16-732-019	FAISAL MOHAMMED	Peketi Ventures
3	1604-16-732-	MOHAMMED ABDUL MALIK	Peketi Ventures

6.5.3

(ITD)

MUFFAKHAM JAH COLLEGE OF ENGINEERING & TECHNOLOGY

INFORMATION TECHNOLOGY DEPARTMENT

22 Oct'2020

CIRCULAR

All the HOD's are hereby informed that "Computational Intelligence: Theory, Implementation & Applications" is being organized by IEEE Computational Intelligence Society Hyderabad Chapteron 22-27 November 2020 which will be conducted in MuffakhamJah College of Engineering & Technology, Hyderabad, India from 22-27 November 2020. So please nominate around 3 faculties from your respective departments. Details of the programme are given below.

Program Title: Computational Intelligence: Theory, Implementation & Applications
Date: 22-27November 2020

30/10/2020

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Dr.Mousmi Ajay Chaurasia

Head -ITD

HEAD
Department of Information Technology
Muffakham Jah College of Engg. & Tech
Road No. 3 Banjara Hills Hyderabad 34

MUFFAKHAM JAH COLLEGE OF ENGINEERING & TECHNOLOGY

INFORMATION TECHNOLOGY DEPARTMENT

22 Nov'2020

CIRCULAR

The participants of the IEEE Summer School (Computational Intelligence: Theory, Implementation & Applications) dated 22-27 November 2020 are informed that every participant is to maintain minimum 70% of attendance to get the programme certificate. If the invigilation is there, before or after the invigilation you have to do the signaturein the attendance sheet on the same day itself.

Dr.Mousmi Ajay Chaurasia

Head –ITD

HEAD
Department of Information Technology
Muffakham Jah College of Engg. & Tech
Road No. 3, Banjara Hills, Hyderabad-34
Tel # +91-40 23392035, Fax : +91-40-23393428

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Joint Chapter of IEEE Computational Intelligence, Geoscience & Remote Sensing Societies
IEEE Hyderabad Section
Presents
6-Day Summer School 2020on
Computational Intelligence: Theory, Implementation & Applications
22-27 November 2020

Venue: MuffakhamJah College of Engineering & Technology, Hyderabad

CHAIRS

AtulNegi, Program Chair, IEEE CIS Summer School 2020

M. Naresh, Program Co-Chair, IEEE CIS Summer School 2020& Chair, CIS/GRSS Jt. Chapter, IEEE Hyderabad Section

The IEEE Computational Intelligence Society Hyderabad Chapter is TWICE identified as the Outstanding CIS Chapter for the year 2013 & 2016. This award is being given for the outstanding contributions to IEEE CIS for the greatest overall contribution and service to its members; the local scientific, professional, governmental, and educational communities; and the IEEE CIS. This recognition served as the motivation for the society to launch IEEE CIS sponsored Summer School in Hyderabad, India. **To organize this CIS Summer school, CIS/GRSS Chapter received the fund of USD 11000 from IEEE Head Quarters.**

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Recent spurt in adoption of computational intelligence based techniques by Industry giants for commercial use has created a demand to reskill the young professionals. Also, many startups that provide computational intelligence based solutions to customers have sprung up and are on lookout for graduate students who have prior exposure and working knowledge in computational intelligence. This in turn has led to a requirement to provide additional skills to new job aspirants. This summer schools attempts to fulfill the above requirements through a balanced program design incorporating theory, implementation and applications of computational intelligence technologies.
We have put together twenty-one lecture sessions, five hands-on sessions and one posterpresentation, all covering a range of topics and areas of interest related to the Evolutionary Computation and Machine Learning with Computational Intelligence (CI) approaches.

Venue: Muffakham Jah College of Engineering & Technology, Hyderabad (M.J.C.E.T) It is located at Banjara hills in the heart of the city and one of the prime locations in Hyderabad. MJCET was established in the year 1980 by Sultan-Ul-Uloom Education Society (S.U.E.S.). This college is affiliated to Osmania University, Hyderabad and approved by AICTE, New Delhi. As per survey of OUTLOOK and WEEK magazine, MJCET was ranked 62nd and 56th respectively among top 100 Engineering colleges in India. Also, it is ranked as one the top five engineering colleges around Hyderabad. There are many good and budgeted hotels nearby and many tourist locations within 56 km radius. MJCET campus is one the most happening places in Hyderabad with many IEEE student chapter activities. It is covered by lush green gardens almost everywhere.

SUMMARY OF SUMMER SCHOOL

A 6-day IEEE Computational Intelligence Society Summer school was conducted at Muffakham Jah College of Engineering & Technology, Hyderabad, India from 22-27 November 2020 on Computational Intelligence: Theory, Implementations & Applications sponsored by IEEE CIS, GRSS and MJCET. A total of 50 participants from various parts of the country had participated. Amongst them, 15 were outstation participants coming from places like Chattisgarh, Uttrakhand, Mumbai, Karnataka, Andra Pradesh etc. The program was widely covered by the press in various local newspapers and dynamic media e.g. Sakshi, Times of India, Namaste Telangana, Andhrajyothi, Eenadu, Deccan Chronicle, Hans-India, Sakshi TV.

This summary is a snapshot of the six-day program in CI consisting of lectures, demonstrations, poster presentation and technology hub local tour visit. In addition to that, two pre events were conducted by CIS volunteers of IEEE Hyderabad Section.

Inaugural session was addressed by:

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- Chief Guest, **Dr. P.N. Suganthan,** Professor, Nanyang Technological University, Singapore
- Guest of Honor **Dr. Sabrina Senatore,** Professor, University of Salerno, Italy
- Welcome address & Introduction to CIS Summer School by **Dr. AtulNegi,** Program Chair
- **Dr. M. Naresh,** Program Co-Chair & Chair, CIS/GRSS Jt. Chapter, IEEE Hyderabad Section
- **Mr. Maruthi Rao,** Chair, IEEE Hyderabad Section
- **Dr. Basheer Ahmed,** Advisor-cum -Director, MJCET
- **Janab Zafar JaveedSahab**, Honorary Secretary, SUES
- Vote of thanks was given by **Mr. P. Laxman Rao,** Program Finance Chair.

The program during the week was hectic, very informative and useful in today's context. All the sessions were highly interactive, lively and interesting and credit goes to all the participants and the speakers. The summer school had 21 presentations that broadly covered the topics specific to Computational Intelligence, Neural Networks, Soft Computing, Fuzzy Logic, Evolutionary Computing, Deep Learning, Gearbox fault tolerance, Machine Learning, Polarimetric SAR Image Analysis, Differential evolution etc.

Eminent Speakers/resource persons across the world were invited during the program.

Some of the eminent resource persons for theory sessions were:

- Dr. P.N. Suganthan, NTU, Singapore
- Dr. J. Sarangapani, Missouri Univ. of Science & Technology, Rolla, USA
- Dr. RistoMiikkulainen, Univ. of Texas, USA
- Dr. Janez Brest, Univ of Maribor, Slovenia
- Dr. M. Pratama, NTU, Singapore
- Dr. Sabrina Senatore, Univ. of Salerno, Italy
- Dr. AnandParey, IIT Indore
- Dr. Akira Hirose, Univ. of Tokyo, Japan
- Dr. Farookh Hussain, Univ. of Technology. Sydney, Australia
- Dr. Avik Bhattacharya, IITB, Mumbai, India
- Dr. Ashish Ghosh, ISI Kolkata, India
- Dr. Alok Singh, Univ. of Hyderabad, India

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Hands-on experience in AI, Machine learning, Fuzzy Logic and AI in Health Care were carried out by the following:

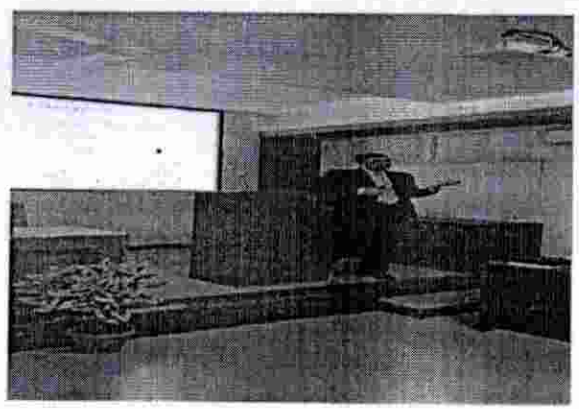
- Dr. Tilottama Goswami, Professor, BVRIT, Hyderabad
- Dr. Srija Katta, Vyas Labs, Hyderabad

On fourth day, a banquet dinner and a cultural program was organized on the theme of Indian cultural. Students performed traditional dance like Bharatanatyam, Kuchipudi and Instruments recital amused the audience. All enjoyed the Indian culture evening.

On last day, Technology hub local tour was arranged for all participants to get the exposure of real time implementation of artificial intelligence, machine learning and other latest technologies.**T-Hub (Telangana Hub)** is India's largest incubator for startups which is headquartered in Hyderabad, Telangana, India.It is community space for start-ups, investors, incubators and accelerators in India.

Finally certificates of participation were presented to all participants.The motive of the program has been successfully achieved and all participants were highly satisfied with the sessions. A raise of 80% membership growth were expected in IEEE CIS and GRSS chapters.Entire organizing team had put all their efforts to set this milestone. Everyone has set their sights high and made every effort leading to grand success.

Some event photos



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HYDERABAD-500 034.(T.S.)

Dr. Mousmi Ajay Chaurasia
Head ITD
HEAD
Department of Information Technology
Muffakham Jah College of Engg. & Tech
Road No. 3, Banjara Hills, Hyderabad 34
Tel# +91-40-23352084 Fax : +91 40 2335 5428

MUFFAKHAM JAH COLLEGE OF ENGINEERING & TECHNOLOGY
INFORMATION TECHNOLOGY DEPARTMENT
Computational Intelligence: Theory, Implementation & Applications
Registration Sheet

S.no.	Name	Designation	Dept.	E-mail	Contact No.
1	Mr. Md. Asrar Ahmed	Asst. Prof.	ITD	asrar.ahmed@mjcollege.ac.in	9704446617
2	Mr.ShaikRasool	Asst. Prof.	ITD	shaikrasool@mjcollege.ac.in	9885633986
3	Mr.MdGouseBaig	Asst. Prof.	ITD	gousebaig@mjcollege.ac.in	9959593404
4	Mr.Mohd Abdul Rasheed	Asst. Prof.	ITD	marasheed@mjcollege.ac.in	9963412526
5	Ms. K Jyothsna	Asst. Prof.	ITD	jyothsna.devi@mjcollege.ac.in	9100225588
6	Mr.KhajaZahooruddin	Asst. Prof.	CSE	zahooruddin@mjcollege.ac.in	9652350351
7	Syed Md. Akbar Hashmi	Asst. Prof.	CSE	akbar.hashmi@mjcollege.ac.in	9394835377
8	SyedaAmbareenRana	Asst. Prof.	CSE	ambareen.rana@mjcollege.ac.in	9908119190
9	ManjushaKalekuri	Asst. Prof.	CSE	manjusha@mjcollege.ac.in	888577133
10	Ms. K. Sridevi	Asst. Prof.	CSE	sridevi@mjcollege.ac.in	9959063991
11	Mohd.NazimRaza	Asst. Prof.	Civil	nazim.raza@mjcollege.ac.in	7207676286
12	SyedaHusnaNooreen	Asst. Prof.	Civil	husna.nooreen@mjcollege.ac.in	953391469
13	N.B.V. Lakshmi Kumari	Asst. Prof.	Mech	lakshmikumari@mjcollege.ac.in	9701734774
14	S. IrfanSadaq	Asst. Prof.	Mech	irfan.sadaq@mjcollege.ac.in	9492572257
15	Hakeem AejazAslam	Asst. Prof.	ECE	aejazaslam@mjcollege.ac.in	9885696755
16	B. Sucharitha	Asst. Prof.	ECE	sucharithanagulapally@mjcollege.ac.in	9490981992
17	Mohammed Imran	Asst. Prof.	EEE	imraneed@mjcollege.ac.in	9885770262
18	Praveen Kumar Joshi	Asst. Prof.	EEE	joshieed@mjcollege.ac.in	8801609130

30/9/22

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Dr.Mousmi Ajay Chaurasia
Head -ITD

HEAD
Department of Information Technology
Muffakham Jah College of Engg. & Tech
Road No. 3, Banjara Hills, Hyderabad-34
Tel # +91 40-23352884 Fax : +91 40-23353428

Muffakham Jah College of Engineering and Technology
Status Report of IQAC Recommendation Activities and Follow-up Actions
[Recommendations: IQAC MoMs dated 31-12-2020 and 20-02-2021]

8-July-2021

S. No.	IQAC Recommendation	Action Taken	Remarks
1.	Introduction of Certificate and Diploma Programs	Proposals submitted by EEE Dept.	
2.	Introduction of Value Added courses imparting transferable and Life skills	Proposal submitted by English Dept. (Pearson MePro)	
3.	Use of ICT for Effective teaching with Learning Management Systems (LMS)	Not Done	
4.	Commissioning of NSS Unit	College NSS Unit formed. Mrs. NBV Laxmi, Asst. Prof. Mech. Dept – Program Officer 10 Faculty Coordinators 200 NSS students	OU Chapter recognition Pending
5.	Capability enhancement and development schemes i. Career Counselling ii. Remedial Coaching	Not Done	
6.	Course on Human Values and Professional ethics	Done	
7.	Workshop/Seminar on Intellectual Property Rights (IPR) and Industry Academia Innovative practices	Done	
8.	Action taken for reflection of faculty publication data on Scopus, Web of Science etc.	Done	
9.	Initiative for registration of Patents	Process Started.	Granted – 01 Published – 03 Filed (Design Patents) - 03
10.	RPS (Research Proposal Scheme), MODROBS (Modernization and Removal of Obsolescence) proposals.	Submitted.	
11.	Registration for National Library and Information Services Infrastructure for Scholarly Content (N-LIST).	Initiated. Faculty Registration done on NDLI portal	

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S. No.	IQAC Recommendation	Action Taken	Remarks
12.	Plan of activities to be conducted as part of Science Day (February 28) Celebrations.	Done	
13.	Seminar on "Human Values and Professional Ethics" by Dr. Soumyajyoti Banerjee, IIM Bodh Gaya.	Conducted on 27th Feb'2021	1. Speaker: Dr. Soumyajyoti Banerjee, Assistant Professor in Communication at Indian Institute of Management Bodh Gaya. 2. Report Awaited
14.	Planning for an annual workshop/ seminar on Intellectual Property Rights (IPR).	To be conducted	
15.	Planning and Execution of COVID19 Awareness related activities by students.	Not Done.	To be executed by College NSS unit.
16.	Constitution of MJCET Alumni Outreach Committee.	7-Member Committee Constituted. Dr. Fahmina Taranum, Prof. CSE Dept.- Coordinator	
17.	Formulation of processes/ procedures for identification and documentation of student progression to higher education (for every outgoing batch).	Not Done	
18.	Formulation of processes/ procedures for identification and documentation of student placements (for every outgoing batch).	To be done.	Responsibility assigned to Placement Coordinator.
19.	Organization and Conduct of 3 Day National Student Web Conference on Trends, Technological Challenges and Innovations in Engineering (TTCIE-2021).	Conducted on 2-4 March 2021	
20.	Proposal for organizing Online HACKATHON 2021.	Deferred	For Academic Year 2021-22
21.	Proposal for organizing Online ADSOPHOS 2021.	Deferred	For Academic Year 2021-22

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S. No.	IQAC Recommendation		Action Taken	Remarks
22.	Activities to be conducted under the aegis of various MJCET Student Chapters.			
	i.	World Water Day (EWB(I) MJCET and EI(I), CED)	Done	
	ii.	No Plastic Day (IEEE and CSI)	To be Done	
	iii.	International Mentoring Day (17-Jan-2021) (Orators Club and ACM)	Event Date Elapsed	

Mrs. Maniza Hijab,
Co-Coordinator IQAC, MJCET.

Prof. Ashfaque Jafari,
Coordinator, IQAC, MJCET.

30/03/2021

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MUFFAKHAM JAH COLLEGE OF ENGINEERING AND TECHNOLOGY

INTERNAL QUALITY ASSURANCE CELL

MINUTES OF THE MEETING HELD ON 20TH FEBRUARY, 2021 AT 11.30 A.M. IN THE SEMINAR HALL

The IQAC meeting was held on 20th February 2021, at 11.30am in MJCET Seminar Hall (Block-IV). The meeting started with Prof. Ashfaque Jafari, Coordinator IQAC MJCET welcoming the IQAC committee members and putting forth the meeting agenda.

Agenda of the Meeting:

1. Action taken for reflection of faculty publication data on Scopus, Web of Science etc.
2. Initiative for registration of Patents.
3. RPS (Research Proposal Scheme), MODROBS (Modernization and Removal of Obsolescence) proposals.
4. Registration for National Library and Information Services Infrastructure for Scholarly Content (N-LIST).
5. Plan of activities to be conducted as part of Science Day (February 28) Celebrations.
6. Seminar on "Human Values and Professional Ethics" by Dr. Soumyajyoti Banerjee, IIM Bodh Gaya.
7. Planning for an annual workshop/ seminar on Intellectual Property Rights (IPR).
8. Planning and Execution of COVID19 Awareness related activities by students.
9. Constitution of MJCET Alumni Outreach Committee.
10. Formulation of processes/ procedures for identification and documentation of student progression to higher education (for every outgoing batch).
11. Formulation of processes/ procedures for identification and documentation of student placements (for every outgoing batch).
12. Organization and Conduct of 3 Day National Student Web Conference on Trends, Technological Challenges and Innovations in Engineering (TTCIE-2021).
13. Proposal for organizing Online HACKATHON 2021.
14. Proposal for organizing Online ADSOPHOS 2021.

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Agenda 1: Prof. Ferhathullah Hussainy, Dean Admin, explained to the members, the importance of faculty publications, citations and their weightage in NAAC grading and NIRF ranking. He reiterated the fact that faculty should get their works published in SCOPUS, Web of Science etc. as these carried weight with ranking agencies. He also listed the current status of faculty members as authors in Publons, the total number of publications, H-index scores etc. Procedure of getting the already published publications listed in Publons and other related aspects was demonstrated.It was resolved to encourage and guide the faculty members to get their works published in journals indexed by these databases.

Agenda 2: Prof. Ishrat M. Mirzana of Mechanical department briefed about the current status of patents granted, published and filed by the college. This was one of the pressing areas that needed attention.

Patents granted	-	01
Patents published	-	03
Design Patents filed	-	03

Further it was informed that for NIRF only institution filed patents are counted, whereas, for NAAC both individual and institution filed patents are counted.

It was decided that projects under taken as part of R&D projects should be encouraged towards patent filing.

Agenda 3: Prof. Ishrat M. Mirzana listed the Research Proposal Schemes (RPS) and MODROB proposal submitted on behalf of the college. RPS were submitted by Civil, CSE and ECE departments while ECE, EEE and IT departments submitted applications under the MODROB scheme. Further MECH and CSE filed application for conduct of ISTE Refresher Course. It was stressed that departments should work to get strong MOUs with industry which would facilitate RPS. Need to look beyond AICTE and SERB for funding was emphasized. Parameters under Faculty capabilities required and the amounts sanctioned were also informed to the members.

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Agenda 4: Mr. Ch. Venkateswarulu, Librarian informed about NLIST and the various access the college gets viz., e-journals, e-books, e-databases etc. All the faculty members were required to get themselves registered by providing their official email-id. Further for Science Direct, Elsevier, IEEE the access was IP based access, hence these could be accessed in college only.

Agenda 5: Dr. M.A. Majeed, Professor and Head of Basic Science & Humanities and Incharge of this year's weeklong Science Day Activities to be conducted from 27th February 2021 spoke about the theme of the celebrations "Future of Science Technology Innovation: Impacts on Education Skills and Work". Different Proposals of activity by each of the departments viz., Mathematics, English, Chemistry and Physics were put forth for discussion and approval. Feedback was to be taken mandatorily and adherence to maintenance of quality and decorum of the events was necessary.

Agenda 6: As part of the Science Day 2021 celebrations, a seminar on "Valuing the Valueless; Ethical Leadership for 21st Century" by Dr. Soumyajyoti Banerjee, IIM Bodh Gaya has been organized. It was decided to through open this seminar and all the webinars to be conducted by the college to all the constituent colleges of the campus with due permission of the Hon. Secretary, SUES.

. Agenda 7: Prof. Ishrat M. Mirzana informed the members that NAAC recognizes one event per year. Further detailed about the training as part of IPR that can be conducted in collaboration with Rajiv Gandhi National Institute of Intellectual Property Management (RGNIIPM) Maharashtra, the type of programs/workshops, number of participants and the related fees.

Agenda 8: It was decided to do the Planning and Execution of COVID19 Awareness related activities by students under NSS unit of the college. Mrs. Lakshmi Kumari, Assistant Professor MECH and the NSS officer of the college would be the Incharge for it.

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Agenda 8.5: Program on IoT under AICTE-INAE DVP Scheme: Prof. Arifuddin Sohel, Head ECE department apprised the members that the department was conducting the above program on IOT as part of AICTE-Indian National Academy of Engineering Distinguished Visiting Professor Scheme, Mr. N. Venkatesh who is a recognized AICTE-INAE DVP and also external guide for ME projects carried out by the students of the college was conducting the sessions with 3 sessions already completed and 4 to be done in the coming week i.e. 22nd Feb 2021.

Agenda 9: A 6-member committee was formed for effective tracking and outreach of the pass out students of the college. Modalities of working to be formulated later. Members of the committee include:

1.	Dr. Fahmina Tarannum,	Associate Professor CSE	- Coordinator.
2.	Mr. Mohd. Masihuddin Siddiqui,	Assistant Professor Civil	- Member
3.	Mrs. Narjis Begum	Assistant Professor EIE	- Member
4.	Mr. Hakeem Aejaz Aslam	Assistant Professor ECE	- Member
5.	Ms. Syeda Romana	Assistant Professor MECH	- Member
6.	Mrs. Gouri R Patil	Associate Professor IT	- Member
7.	Dr. Gitasri Mukherjee	Associate Professor English	- Member

Agenda 10: Prof. Arifuddin Sohel was authorized by the members to do a survey of other colleges for this activity, form a committee and submit a report.

Agenda 11: Placement officer Mrs. Rajini was asked to look into it.

Agenda 12. Mr. Zainuddin Naveed, Assistant Professor CSE and member TTCIE 2021 briefed the members that the web based conference TTCIE 2021 was to be conducted between 2nd - 4th March 2021. He also informed about the schedules of this student conference, number of paper submissions received, the submission and the reviewing process through easychair conference management system, the 3 virtual workshops conducted by Prof. Ferhathullah Hussainy, Mr. Ahmed and Prof. Ishrat for the participating students. A total of 134 paper submissions with 7 from outside

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were received out of which 2 were rejected and 1 withdrawn. Heads of department were asked to nominate 2 faculty members for the reviewing process.

Agenda 13: Mr. Zainuddin Naveed put before the members that this is the 8th in row Hackathon to be conducted by the college. Tentatively it was proposed to conduct in the 1st week of June.

Agenda 14: In view of the COVID19 pandemic and the laid down SOP, it was decided to conduct ADSOPHOS in the next semester.

Agenda 14.5: Proposal for organizing the following events by the respective student bodies was proposed and approved.

- World Water Day (March 22, 2021) to be organized by EWB (I) MJCET Student Chapter EI(I) Student Chapter – Civil Engineering.
- No Plastic Day (July 3, 2021) to be organized by IEEE and CSI
- International Mentoring Day (January 17) whose day has elapsed to be conducted by the Orators Club and ACM student chapter.

The meeting concluded with the coordinator thanking the members.

8/3/21
Mrs. Maniza Hijab
Co-coordinator, IQAC

8/3/21
Dean Academics
Cordinator, IQAC

Advisor cum Director
Chairperson, IQAC

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MUFFAKHAM JAH COLLEGE OF ENGINEERING AND TECHNOLOGY

ACADEMIC AUDIT

Inspection Performa for Quality of Evaluation of Theory Courses

Academic Year: 2020-2021

Name of the Course: Computer Aided Modelling and Design Course Code: PC 510/CD Semester: I/II

Name of the Faculty: Dr. Ishrat M.M Department: Mechanical / Production ME CAD/CAM

Department for which course is offered: ME CAD/CAM. Class: I/II/III/IV Sec: A/B

S.No	Parameter	Comments
1	Student Roll No	Yes
2	Schedule of Classes (time Table)	Yes
3	Syllabus	Yes
4	Course Handout	Yes
5	Teaching Schedule	Yes
6	Assessment Plan	Yes
7	Assignment with Key	Yes (online)
8	Tutorials / Quiz etc. with Key	—
9	Question Papers of Class test 1 & 2 with Key	Yes
10	OU Question Paper with Key	Yes
11	Sample Copies (Best / Average / Worst) of Assignment	Yes. (online)
12	Sample Copies (Best / Average / Worst) of Tutorial / Quiz	—
13	Sample Copies (Best / Average / Worst) of Class test paper	Yes (online)
14	Course End Survey	Yes
15	University Results of Past 5 Years	Yes
16	Assessment Matrix – CO wise	Yes
17	Topic Covered under Content Beyond the Syllabus	—
18	Course Closure Report	Yes

Any Other Suggestions:

Faculty Signature **Signature of Academic Audit Committee Chair**

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MUFFAKHAM JAH COLLEGE OF ENGINEERING AND TECHNOLOGY

ACADEMIC AUDIT

Inspection Performa for Quality of Evaluation of Laboratory Courses

Academic Year: 2020-2021

Name of the Course: Advanced CAD lab Course Code: PC515ME Semester: I/II

Name of the Faculty: Dr Ishrat MM Department: Mechanical / Production

Department for which course is offered: ME CAD/CAM Class: I/II/III/IV Sec: A/B

S.No	Parameter	Comments
1	No. of Experiments Planned as per syllabus	Yes
2	No. of Experiments Conducted as per syllabus	Yes
3	Review of Laboratory Assessment Sheets	Online
4	Availability of Laboratory Manuals as per syllabus	Yes
5	Inspection of Laboratory Records evaluation	Yes
6	Inspection of Log Book	—
7	Evaluation of Internal Test& Viva VOce	Yes.

Signature of Faculty

Signature of Academic Audit Committee Chair

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S.L. No. 3234 Dt. 09/06/2020

Sold To Dr. Basheer Ahmed

S/o. W/o. D/o. Late. Abdul Latef

To Whom Self

K. VINAY KRISHNA
LICENSED STAMP VENDOR
L. No.16-04-027/2017
R.L.No.16-04-070/2020
H.No: 8-2-245/1/7/25, ROAD No: 1,
BANJARA HILLS, HYDERABAD-82.
Mobile Number: 9849383123

Memorandum of Understanding
between
M/s. Binford Research Labs Private Ltd., Hyderabad, Telangana
and
Muffakham Jah College of Engineering and Technology, Hyderabad, Telangana
on
Cooperation in Research, Innovation & Internship

M/s. Binford Research Labs Private Ltd., Hyderabad, Telanagan State
And Muffakham Jah College of Engineering and Technology, Telangana State
(Hereinafter referred to as "the Participants"),

For Binford Research & Labs Pvt. Ltd.

(Mr. Bhimsetty Sidhanth) Director
DIRECTOR,
M/s. Binford Research Labs Pvt. Ltd.,
HYDERABAD.

(Dr. Basheer Ahmed)
ADVISOR CUM DIRECTOR
Muffakham Jah College of Engg. & Tech,
HYDERABAD.

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Banjara Hills, Road No. 3,
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ADVISOR-CUM-DIRECTOR
Muffakham Jah College of
Engineering & Technology
Road No: 3, Banjara Hills,
Hyderabad - 500 034.(A.P.)

This Memorandum of understanding is made and executed on 5th day of December, 2020 at Hyderabad by and between:

1] M/s. BINFORD RESEARCH LABS PRIVATE LTD,
Having its Regd. Office at 5-5/137, Rajalingam Colony, Boduppal, Hyderabad – 500 092, Telangana State., Rep. by its Director, Bhimisetty Sidhanth.

Hereinafter referred to as the Party of the First Part [which term shall mean and include all its heirs, assigns, successors in interest, legal representatives, etc.]

2] MUFFAKHAM JAH COLLEGE OF ENGINEERING AND TECHNOLOGY,
Rd Number 3, Venkateshwara Hills, Banjara Hills, Hyderabad - 500034, Telangana, India., hereinafter referred to as "MJCET", Rep. by its Advisor cum Director, Dr. Basheer Ahmed.

Hereinafter referred to as the Party of the Second Part [which term shall mean and include all its heirs, assigns, successors in interest, legal representatives, etc.]

WHEREAS, the party of the First Part is actively pursuing Research & Development in the area of indigenous drones to increase self-reliance for India and reduce the Defendant on external companies in other countries.

WHEREAS, in furtherance of the same, the Company has established to make Robust Hardware and Software products related to Robotics and Unmanned aerial vehicles, and the party of the First Part has been collaborating with the Government, Regulatory Authority and other experts in the said field.

WHEREAS, unmanned aerial vehicles also known as UAVs or drones have decentralized air space access, allowing agriculturists, construction workers and other civilian users to integrate areal monitoring into their daily work.

WHEREAS, advancements in the fields such as automation, robotics, miniaturization, materials science, spectral and thermal imaging have resulted in drown enabled solution in areas as diverse as the agricultural, power, infrastructure and telecom structures as well as crowd and Disaster Management.

For Binford Research & Labs Pvt. Ltd.

(Mr. Bhimsetty Sidhanth)
DIRECTOR,
M/s. Binford Research Labs Pvt. Ltd.,
HYDERABAD.

Director

(Dr. Basheer Ahmed)
ADVISOR CUM DIRECTOR
Muffakham Jah College of Engg. & Tech,
HYDERABAD.

ADVISOR-CUM-DIRECTOR
Muffakham Jah College of Engineering & Technology
Road No: 3, Banjara Hills,
Hyderabad - 500 034.(A.P.)

PRINCIPAL
Muffakham Jah College Of Engineering & Technology
Banjara Hills, Road No. 3,
HYDERABAD-500 034 (T.S.)

WHEREAS, party of the Second Part is an Institute of Technology and imparts education in various fields of technology.

AND WHEREAS, both the parties hereto are desirous of entering into this Memorandum of Understanding on research, product R & D and Internship.

NOW THEREFORE THIS MEMORANDUM OF UNDERSTANDING WITNESSETH AS FOLLOWS

That, the party of the First Part would be developing various products relating to drones and would be developing hardware and software, necessary for proper functioning of the drones.

That the party of the First Part would be sending the products that the party of the First Part would be developing for further sophistication of the said product by the party of the Second Part.

That the party of the First Part would be providing necessary Engineering support and requisite parts if need be.

That the party of the Second Part would use their infrastructure, faculty and students do tangible research work on the product with the party of the First Part sends to the party of the Second Part.

That the party of the Second Part will get a royalty on any product that the party of the First Part, commercializes which has been completely developed with the help of the party of the Second Part.

That if both the parties to this MOU apply for any grant together, a portion of the grant will be made available to the party of the First Part in the form of R & D budget which the party of the Second Part raises on joint work done by the parties to this MOU together.

That the party of the First Part can provide the party of the Second Part with certain drone components required which will be used solely for research purposes.

For Binford Research & Labs Pvt. Ltd.

Director

(Mr. Bhimsetty Sidhanth)
DIRECTOR,
M/s. Binford Research Labs Pvt. Ltd.,
HYDERABAD.

(Dr. Basheer Ahmed)
ADVISOR CUM DIRECTOR
Muffakham Jah College of Engg. & Tech,
HYDERABAD.

ADVISOR-CUM-DIRECTOR
Muffakham Jah College of
Engineering & Technology
Road No. 3, Banjara Hills,
Hyderabad - 500 034.(A.P.)

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That the party of the Second Part will provide the party of the First Part research expertise and the party of the First Part shall provide Industry expertise to the party of the Second Part.

That the students of the party of the Second Part from 2nd year to Ph.D. can apply for internship with the party of the First Part when any research and development work done during the said internship period would be confidential and would be exclusively owned by party of the First Part.

That any development, improvement or modifications of equipment, service parts, design, manufacturing drawings and IPR related shall be inclusive for both the parties.

That the parties to this MOU covenant that any technical knowhow, ideas, materials, business information shall be kept purely confidential and shall not be disclosed to any other persons except with the prior approval of the other party to this MOU.

That both the parties to this MOU further covenant that neither of the parties shall be liable for loss, damage, detention or delay nor be deemed to be in default for failure to perform when prevented from doing so by causes beyond its reasonable control such as acts of god, fire, strike or omissions of any Governmental authorities or Governmental regulations.

For Binford Research & Labs Pvt. Ltd.

(Mr. Bhimsetty Sidhanth)
Director
DIRECTOR,
M/s. Binford Research Labs Pvt. Ltd.,
HYDERABAD.

(Dr. Basheer Ahmed)
ADVISOR CUM DIRECTOR
Muffakham Jah College of Engg. & Tech,
HYDERABAD.

ADVISOR-CUM-DIRECTOR
Muffakham Jah College of
Engineering & Technology
Road No: 3, Banjara Hills,
Hyderabad - 500 034.(A.P.)

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SIC-TPG for path delay fault detection in VLSI circuits using scan insertion method

Sabir Hussain M A Raheem[2] and Afaq Ahmed[3]
[1,2] Associate Professor, ECED Muffakham Jah college of Engineering and technology Hyderabad, India
[3]Professor, Department of Electrical and Computer Engineering, Sultan Qaboos University, Oman
sabir.mj@gmail.com[#1] abdulraheem@ieee.org[#2] afaq@squ.edu.om[#3]

Abstract*— The advent of deep submicron technology led to growing complexity of circuits and an increase in the design speed, making delay testing necessary for determining correct circuit behavior. Observation of path delay faults requires propagation of transitions in a circuit which is done by application of pair of patterns. This paper proposes a single input change test pattern generator (SIC- TPG) that creates SIC pairs and hence can be used for path delay fault detection. The same TPG also senses stuck-at faults in circuits. A path definition file is specified for benchmark circuit and mentor graphics fastscan tool is used to obtain the fault coverage. For the purpose of area overhead comparison, the TPG is coded in verilog and simulated by Xilinx ISE simulator and improved results are observed. Experiments conducted on ISCAS-85 and ISCAS-89 benchmarks show high stuck-at fault coverage and Path Delay Fault (PDF) coverage.

Keywords — SIC-TPG, Low power BIST, Path delay faults, path description file.

I. INTRODUCTION

Owing to the drawbacks of external Automatic test equipment (ATE) like expensive testing, increased test data volume and test application time, Built-in-self test (BIST) technique, that designs additional hardware and software features into an integrated circuit (IC) thereby allowing them to perform self-test, are being used extensively. BIST consists of a test-pattern generator (TPG) that applies test vectors to a given circuit under test (CUT) for the purpose of fault detection.

Many TPGs detect stuck-at faults in circuits and are able to achieve high fault coverage but they are unable to detect physical defects in circuits. Testing of physical defects like stuck-open faults in CMOS and path delay faults requires a TPG that generates a pair of patterns [1]. The two-pattern test TPGs can be single input change (SIC) or multiple input change (MIC), however SIC pairs are mostly preferred because of minimum transition, uniform distribution and uniqueness of patterns and therefore can also be used for low power applications.

Various TPGs have been proposed for generating two patterns test vectors for path delay fault detection. A reconfigurable Johnson counter based TPG generates multiple SIC pattern in test per scan scheme [2] and both test- per-scan and test-per clock scheme [3]. SIC pairs are generated in $nx2^n$ cycles using decoder based SIC pair generator (DSG) algorithm [4] and by applying T transformation to the output of gray coder [5]. Testing multiple modules with $2^n x(2^n - 1)$ two-pattern pairs is done by modifying control logic of the accumulator based TPG in [6]. A pseudo-random pattern generator (RPG) and a scan shift register (SSR) based TPG [7] is used for delay fault testability of array multiplier. A heuristic-driven TPG procedure that generates a robust test for simultaneously detecting maximum possible path faults is given in [8]. A graph approach for tracing paths is presented in [9] where the same TPG detects both stuck-at and path delay faults. Delay faults testing in [10] is done by changing sequential circuits into pseudo sequential and randomly choosing paths between inputs and outputs.

In this paper, a single-input change test pattern generator (SIC-TPG) that generates two pattern test vectors is proposed such that the TPG detects stuck-at faults and also be used for detecting path delay faults. After specifying the paths of CUT in a path description file, the path delay fault coverage canbe calculated by application of patterns.

The rest of the paper is ordered as follows. Section II presents the SIC-TPG. Section III explains the path delay faults and their calculation. Section IV briefs stuck-at faults and their calculation. Section V gives simulated results and synthesis report of TPG. Section VI concludes the paper.

II. SIC TEST PATTERN GENERATOR(SIC-TPG)

LFSR is extensively used as TPG because of its small circuit area and good stuck-at-fault detection, however randomness of patterns generated by LFSR significantly decreases connection among test vectors thereby increasing test power. Fig. 1 shows a 5-bit LFSR.

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LFSR are also incapable of generating two pattern test vectors which are essential requirement for detecting stuck-open and delay faults.

Because of the above-mentioned disadvantages of LFSR, a SIC TPG is proposed which generates single-input changing pair of test patterns thereby being able to detect sequential faults.

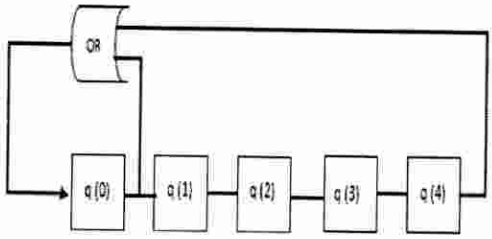

Figure 1 . LFSR for 5 -bits

A. Advantages of using SIC-TPG:

- SIC TPG generate patterns such that consecutive patterns vary exactly in one bit.
- The TPG can be used for low power applications because of reduced switching activity.
- Generation of SIC pairs allows stuck-open and delay fault detection.

B. SIC Generator (SICG):

SICG shown in fig.2. consists of a n-stage counter followed by gray encoder circuit. The gray encoder is used to encode the counter's output so that successive values of its output G[n-1:0] differ only in one bit.

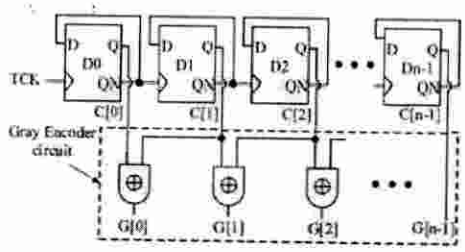

Figure. 2 SICG

$$G[0] = C[0] \text{ XOR } C[1]$$

$$G[1] = C[1] \text{ XOR } C[2]$$

$$G[2] = C[2] \text{ XOR } C[3]$$

.....

$$G[n-2] = C[n-2] \text{ XOR } C[n-1]$$

$$G[n-1] = C[n-1]$$

C. Working

SIC-TPG consists of a single input changing generator (SICG), a barrel shifter, a k-stage counter and a k-to-n decoder, a k-input OR gate and a series of XOR gates as shown in fig.3. Its operation is explained below:

Initially, the SIC-TPG is reset thereby resetting all the internal modules. Next the SICG which consists of a counter followed by gray encoder produces sequence {G[n-1], G[n-2],.....,G[0]} which appears directly at output without shifting and being XORed with decoder output. After the SICG counter reaches its maximum value i.e. counts till 2^n-1 then the k-stage counter increases to 1.

Now the output of SICG is shifted one position to the right by the barrel shifter and then is XORed with decoder output 0000....01 generating sequence {G'[n-1],G[0],G[1],....G[n-3],G'[n-2]}. When this completes, the k-stage counter is again incremented by 1 thus SICG output is shifted by 2-bits and XORed with decoder output 0000....010 thereby generating sequence {G[n-2],G'[n-1],G[0],....G'[n-3]} and so on.

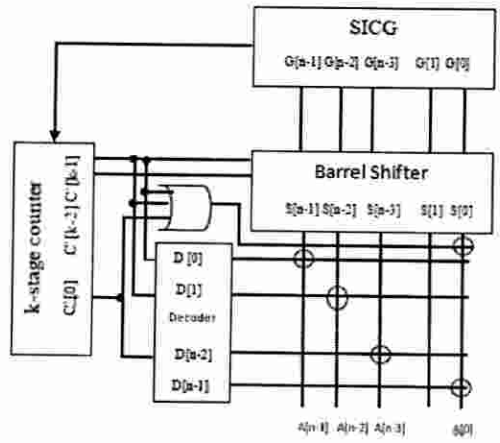

Figure. 3 . SIC- TPG

After obtaining the patterns they are applied to given circuit under test (CUT) for testing and obtaining the fault coverage using mentor graphics fastscan tool.

D. Circuit Under Test (CUT):

For the purpose of comparison in the area of test generation, International Symposium for Circuits and Systems (ISCAS) circuits are used as CUTS.

ISCAS-85 benchmark circuits are combinational circuits and ISCAS-89 benchmark circuits are sequential circuits.C17 circuit is a combinational benchmark circuit with 5 inputs, 2 outputs and 6 two-input NAND gates as shown in Fig. 4.

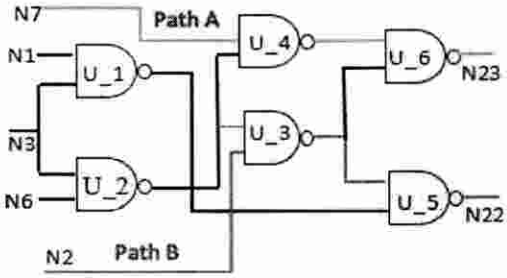

Figure. 4 . C 17 Benchmark

III. PATH DELAY FAULT MODELLING

With the decreasing feature size, delay faults are becoming more widespread. Path delay fault model reports defects that are spread across several gates. If the delay of any of the paths in a circuit exceeds specified limit then that circuit is said to be a faulty circuit. With the total number of paths in a circuit being an exponential function of gates, the detection of path delay faults becomes complicated for large circuits.

For detecting path delay faults in a circuit, pair of vectors V = {V1, V2} needs to be applied such that the first vector initializes relevant internal signals to desired initial logic values, while the second vector causes desired transitions and sensitizes the transition from the target fault site to an output. Here the path delay faults are calculated for C17 combinational benchmark circuit by applying the multiple single input change patterns generated by SIC TPG.

Path delay faults for C17 circuit are calculated using the mentor graphics fastscan tool. The inputs for the tool are gate level netlist of C17 circuit, an ATPG library, path description file and external pattern file which contains all the $nx2^n$ single input changing patterns. The output of the tool is the obtained fault coverage.

A. Path Description File:

Path description file is an ASCII file which defines all the paths in a circuit that are to be tested. An example of path file for C17 circuit in fig.4 for two paths is shown in fig. 5.

The statements of the file include:

- Path: A unique pathname for a path is assigned with this statement e.g. pathA and pathB shown in fig. 5.
- Pin: This statement identifies a pin in the path by its full pin pathname. In "pathA", one pin pathname is "/U4/OUT". The pin pathnames must be ordered from primary input to primary output. A "+" or "-" after the pin pathname indicates the inversion of the pin with respect to the launch point.
- End: A statement that specifies completion of the current path.

```
PATH "pathA" =
PIN /N7 +;
PIN /U_4/OUT +;
PIN /vin_7/OUT -;
PIN /U_6/OUT -;
PIN /vin_11/OUT -;
END;
PATH "pathB" =
PIN /N2 +;
PIN /U_3/OUT +;
PIN /vin_5/OUT -;
PIN /U_5/OUT -;
PIN /vin_9/OUT +;
```

Figure. 5 . Path description file

B. Path delay fault coverage

The path delay fault coverage can be calculated using the steps explained in Fig. 6.

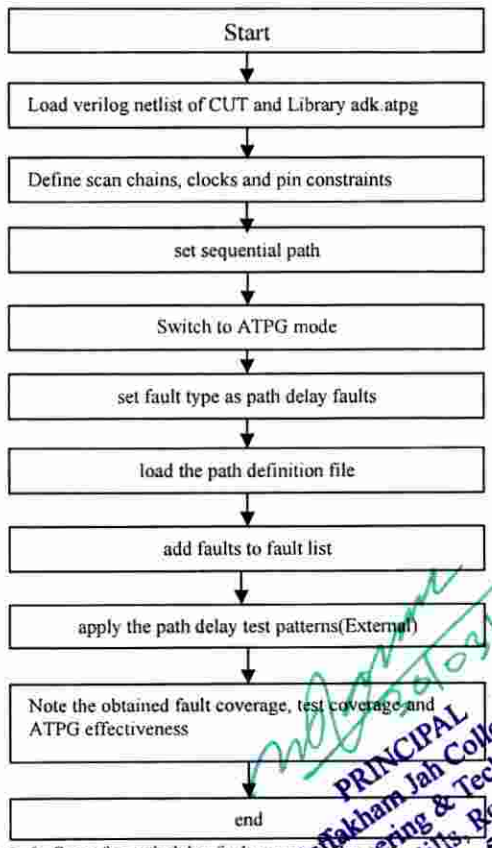

Figure. 6 . Steps for path delay fault coverage flow

First the fastscan is invoked and the tool goes into setup mode. After loading the Verilog netlist and library for given CUT, timing information is loaded using the test procedure file. Next the system mode is set to ATPG and the fault type is path delay faults. Loading the path description file and adding fault sites is done next. The proposed SIC TPG patterns are then applied to obtain the fault coverage.

A total of 5 paths were written in the path description file and 80 SIC TPG patterns were simulated to achieve a path delay fault coverage of 100% for C17 circuit as shown in fig. 7.

```
            Statistics Report
            Path-delay Faults
-----------------------------------------
Fault Classes                   #faults
                                (total)
--------------------------  --------------
  FU (full)                       32
  ------------------------  --------------
  DR (det_robust)               32 (100.00%)
-----------------------------------------
Coverage
  ------------------------
  test_coverage                 100.00%
  fault_coverage                100.00%
  atpg_effectiveness            100.00%
-----------------------------------------
#test_patterns                      18
  #clock_sequential_patterns        18
#simulated_patterns                 18
CPU_time (secs)                   0.3
-----------------------------------------
```

Figure. 7 . Path delay fault coverage

C. *Path Description File*

A stuck-at fault alters the correct value on the faulty signal line to appear to be stuck at a constant logic value. If the signal line is stuck to logic 0 (logic 1), it is called as stuck-at-0 (stuck-at-1) fault. A circuit with n nets can have 2n stuck-at-faults.

A simple example of AND gate with its input "a" stuck-at-0 shown in fig. 8. Results in output "Y" being "0" instead of "1".

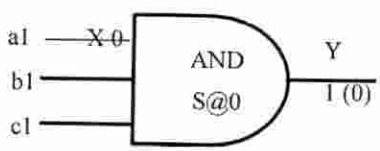

Figure. 8 . AND Gate stuck-at-0

D. *Stuck-at-fault Coverage*

The measurement of stuck at faults have been considered to show the effectiveness of proposed TPG compared with path delay fault modeling, the gate level netlist of circuit under test and the ATPG library is given as input to tool and the output statistics report indicates the calculated fault coverage.

The sample statistics report obtained for C17 benchmark circuit for 74 faults when the SIC TPG patterns are applied is shown in fig. 9.

```
          Statistics Report
          Stuck-at Faults
-----------------------------------------
Fault Classes                   #faults
                                (total)
--------------------  --------------
  FU (full)                       74
  --------------------  --------------
  DS (det_simulation)           74 (100.00%)
-----------------------------------------
Coverage
  ------------------
  test_coverage                 100.00%
  fault_coverage                100.00%
  atpg_effectiveness            100.00%
-----------------------------------------
#test_patterns                      7
#simulated_patterns                32
CPU_time (secs)                   1.2
```

Figure. 9 . Stuck-at-fault coverage for C 17 circuit

IV. EXPRIMENTAL RESULTS

The proposed SIC TPG was simulated on Xilinx ISE simulator and its patterns obtained are verified with the theoretically generated patterns. Simulation results are shown in fig. 10. Table I shows the area and delay comparison of TPG with those proposed in [2] and also the fault coverage for c880 circuit.

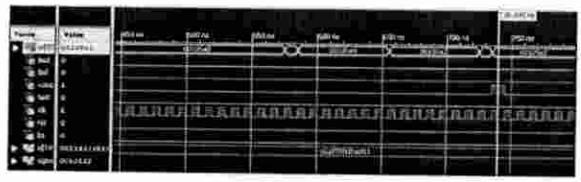

Figure 10 . Simulation Result of SIC TPG

TABLE I. Comparison of synthesis report

Parameter	MSIC TPG [2]	Accumulator TPG [2]	Proposed SIC TPG
Registers	464	146	25
LUT	708	389	78
Global clock buffer	6	1	1
IO	9	3	11
Delay (ns)	7.326	6.881	6.603
Fault coverage	99%	95%	99.83%

From the synthesis report, it is observed that SIC-TPG has less area and delay compared to MSIC and accumulator TPG while also achieving comparable fault coverage.

The stuck-at fault coverage is calculated for ISCAS-85 and ISCAS-89 benchmarks circuits using SIC TPG patterns which is in the range of 89% to 100%

and Path delay fault (PDF) coverage have been implemented by increasing number of fault locations and achieved 92 % to 100% fault coverage shown in Table II

II.TABLE II. Path Delay fault Coverage (PDFC)

Benchmark Circuit	No. of faults	Fault Coverage (FC %)
C17	1074	99.9
C432	2078	97.38
S344	1282	99.83
S27	2106	96.28
S382	9800	98.50
S1488	7000	90.93
S298	836	90.94
S400	900	95.25
74181	567	92.22
74182	208	97.26

V. CONCLUSION AND FUTURE SCOPE

The proposed SIC-TPG is found effective in detecting path delay faults apart from the usual detection of stuck-at faults. Experimental results show Path Delay fault coverage between 92% to 100% for stuck for combination and sequential benchmarks. The Proposed TPG also has less area and delay when compared with MSIC and accumulator based TPGs. From the synthesis report, it is observed that SIC- TPG has less area and delay (ns) reduced to 9.5% and 4% compared to MSIC and accumulator TPG respectively. This work leads to several exciting research directions, Fault modeling of Hard to detect faults and Bridging faults that form a significant class of stable faults may not be modeled as stuck faults like s_a_0 and s_a_1, while delay faults were considered, hard to detect faults and bridging faults can also be targeted using this TPG. The proposed techniques may be used for RAM testing.

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A low power low ripple Schmitt trigger based PWM Boost Converter for Energy Harvesting Applications

Salma Khan, Syed Azeemuddin
Center for VLSI and Embedded Systems
International Institute of Information Technology
Hyderabad, India
Email:salma.khan@research.iiit.ac.in

Mohammed Arifuddin Sohel
Electronics and Communication Engineering
Muffakham Jah College of Engineering and Technology
Hyderabad, India
Email:arif.sohel@mjcollege.ac.in

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***Abstract*—The design of monolithic power management circuits is critical in energy harvesting applications. A Pulse width modulation (PWM) boost converter with feedforward and feedback control mitigates the changes in input-output parameters and avoids the use of compensation circuit. However, the conventional design of a clock generator in feedback path employs power hungry comparators and latches. This paper proposes an improved design of clock generator replacing comparators and latches with a schmitt trigger circuit. As a result, a low power and a low ripple PWM was acheived. The design was implemented in UMC 180 nm CMOS technology generating a stable output of 3.3 V for an input range of 1.2 V - 1.6 V. Due to the application of the proposed technique, a reduced power consumption of 60.19 mW and low ripple voltage of 18.29 mV was achieved, for a maximum load current of 100 mA at an efficiency of 98%. Thus making the design suitable for energy harvesting applications.**

***Index Terms*—Energy Harvesting, Power management, PWM Boost Converter, Schmitt Trigger**

I. Introduction

Energy harvesting is emerging as the key research area for low-power applications in battery driven devices used in medical equipments, consumer electronics, wearable electronics and military applications. The design of power management unit for energy harvesting applications is heavily dependent on the efficient design of the boost converter. Pulse width modulation (PWM) based boost converters have been widely implemented due to the simplicity and compactness of design [1]–[3]. These PWM based converters can be classified into voltage, current and hysteresis controlled converters. The converters based on current control technique are complicated and are difficult to stabilize. Whereas, the voltage controlled boost converters are relatively straight-forward but the output stability is dependent on the compensation circuit [2]. This compensation circuit is circumvented by using a feedforward and feedback loop control thus making the circuit more agile. Using this compensation free technique, a boost converter was designed employing a ramp based clock generator consisting of two hysteresis comparators and one SR latch [3]. Yet, this circuit gives a ripple of 36.52 mV with 93% efficiency and power dissipation of 348 mW. Even though this work is able to eliminate the compensation circuit, it has a power consumption of the order of hundreds of milli watts and is also area hungry.

The problem of area and power can be resolved by using a schmitt trigger for designing ramp based clock generator [4]. In this paper, it is proposed to use the aforementioned ramp based clock generator to design a PWM based boost converter which consumes low power and low area. The effective power consumption is reduced to the order of 10's of milliwatts, with good line and load regulation. The proposed boost converter is designed for an input voltage range of 1.2 V - 1.6 V generating a stable output voltage of 3.3 V with a load current of 100 mA. Design aspects that are commonly used is the provision of the back gate diode which is connected across the switching transistor [5]. Ripple voltage and efficiency are also key factors governing the design of a low power DC-DC converter [6]. Any changes in the input voltage results in a corresponding change in the output voltage which is balanced by the feedback mechanism to bring stability to the output. The generation of a ramp signal from a fixed duty cycle clock pulse was described in [7] and has been further enhanced in [8] and the same is applied in the proposed design. These specifications are suitable for the design of an energy harvesting circuit aimed at driving a wireless sensor node [9].The detailed circuit description of feedforward and feedback circuit along with the proposed design of boost converter using ramp based clock generator with Schmitt trigger circuit is elucidated in section II. The design results are discussed in section III and conclusion is presented in section IV.

II. Circuit Description of Feedforward and Feedback Control of Boost Converter

The circuit consists of Ramp based Clock Generator, Hysteresis Comparator, Level Shifter and Non Overlapping Clock Buffer as per the schematic shown in Figure 1. It depicts the circuit design of the boost converter with feedforward and feedback control circuitry. The forward path consist of the power stage having inductor (L), MOS switches (MN0 & MP0) and load capacitance (C_L). The voltage divider circuit at the input stage consisting of R_{FF1} and R_{FF2} are used to generate voltage V_H given to the non-inverting terminal of hysteresis comparator forming the feedforward path. The output of hysteresis comparator is given to a level shifter

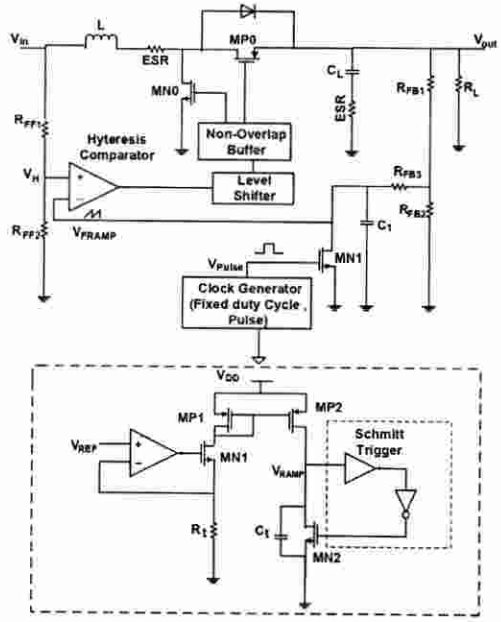

Fig. 1. PWM based Boost Converter

that is connected to a non-overlapping buffer which finally generates the pulse signals that control the switching action of MP0 and MN0. The voltage divider R_{FB1} and R_{FB2} samples the output voltage and is given to the capacitor (C_1) through R_{FB3}. The crucial component in this design is the transistor MN1 which is responsible for charging and discharging of the capacitor (C_1) to generate a ramp signal. This ramp signal is given to the inverting terminal of hysteresis comparator to complete the feedback loop. The frequency of the ramp signal is controlled by the clock generator.

The Clock generator consists of a PMOS current mirror using MP1 and MP2. The MN1 transistor is connected through a two stage operational amplifier connected in the active cascode mode to increase gain of the transistor. The transistor MN2 controls the switching action of capacitor (C_t), thus generating the ramp signal. The frequency of this ramp signal can be adjusted by the schmitt trigger and inverter, depicted in the red box, connected in the feedback loop to the gate of the transistor MN2.

The detailed schematic of clock generator predominantly consists of a Schmitt trigger circuit as shown in Figure 2, which converts the ramp signal into a pulse signal. The frequency of the generator can be measured with reference to Upper Trigger Point (UTP) and Lower Trigger Point (LTP) of Schmitt trigger circuit. It consists of three PMOS and three NMOS transistors. The two PMOS transistors (M_{U1} and M_{U2}) and two NMOS transistors (M_{L1} and M_{L2}) are fed with a ramp input [10]. As the ramp voltage is rising from 0V, the bottom two transistors (M_{L1} and M_{L2}) are off and output is at high level. When the ramp voltage rises to a value greater than the voltage required to turn bottom transistor ON, the output switches to low voltage at this UTP. Similarly the LTP can be obtained in the reverse direction. The transistor aspect ratio(W/L) can be varied to control the UTP and LTP and the same is governed by equation (1) and (2),

$$\frac{K_{L1}}{K_{L3}} = \left\{ \frac{V_{DD} - V_{UTP}}{V_{UTP} - V_{TN}} \right\}^2 \tag{1}$$

$$\frac{K_{U1}}{K_{U2}} = \left\{ \frac{V_{LTP}}{V_{DD} - V_{LTP} - |V_{TP}|} \right\}^2 \tag{2}$$

The frequency of operation which is based on resistor (R_t), capacitor (C_t) and reference voltage (V_{REF}) of the ramp based clock generator is given in equation (3),

$$f = \frac{V_{REF}}{R_t C_t (V_{UTP} - V_{LTP})} \tag{3}$$

In this paper, this modified ramp based clock generator is used to implement the boost converter as shown in Figure 1. Thus automatically reducing the overhead of two hysteresis comparators and SR latch. Based on this contribution, this design achieves reduced power consumption of 60.19 mW when compared to the earlier value of 348 mW [3].

III. RESULTS AND DISCUSSIONS

The simulation results of the proposed boost converter is shown in Figure 3. The output stabilizes at a value of 3.37 V with a ripple of 18.29 mV after a transient time of 88 usec for an input voltage of 1.6 V.

The clock frequency of the circuit is 730 KHz with maximum output load current 100 mA and the ripple voltage is noted as 18.29 mV as shown in Figure 4. The duty cycle of the clock signal is based on both the feedforward and feedback components and any changes in the input and subsequent changes in the output will be balanced out by this mechanism to maintain a stable output voltage of 3.3 V.

The line regulation is performed at full load condition (I_L = 100 mA) with the input range of 1.2 V - 1.6 V and the output is depicted in Figure 5, which indicates a stabilized voltage of 3.3 V with line regulation of 235 mV/V. The input voltage is changed from 1.2 to 1.6 V at 0.4 msec and from 1.6 to 1.2 V at 0.75 msec.

The Figure 6 depicts stable performance of the boost converter for both light load (10 mA) and heavy load (100 mA) at an input voltage of 1.4 V, thus giving a load of regulation 10 mV/mA.

The power consumption of this circuit is 60.19 mW. It is observed that the duty cycle of the clock signal is 65%. Using the equation (4), and substituting the values of V_{out} to be 3.37 V and $V_{in(min)}$ to be 1.2 V, the efficiency of this circuit is calculated to be 98%.

$$Efficiency = \frac{V_{out}(1-D)}{V_{in}} \tag{4}$$

It is evident from Table I that the variation of important design parameters with respect to corner conditions is marginal and the proposed design is stable at the process corners.

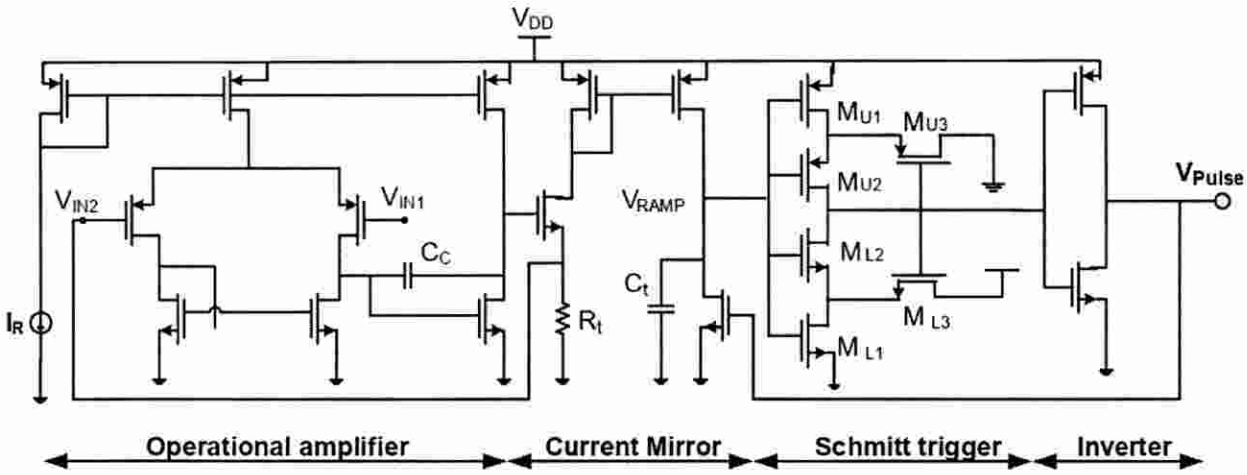

Fig. 2. Detailed schematic of proposed clock generator

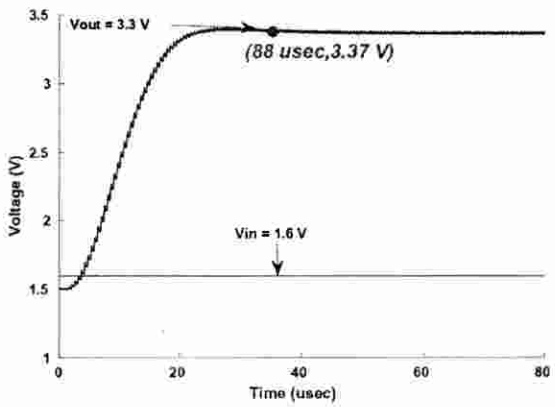

Fig. 3. Transient analysis of boost converter

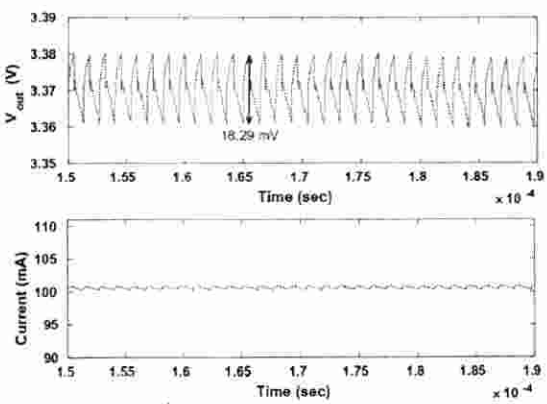

Fig. 4. Ripple voltage and load current

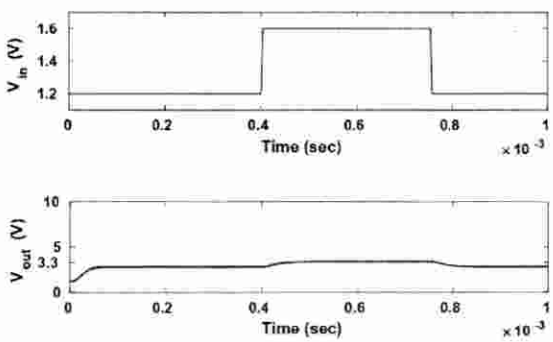

Fig. 5. Line Regulation.

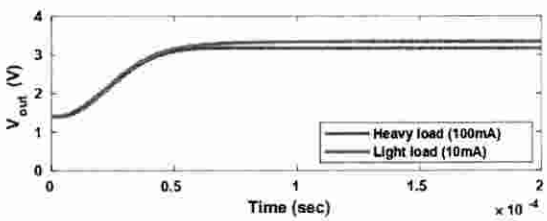

Fig. 6. Load Regulation.

TABLE I
SIMULATION RESULTS FOR CORNER CONDITIONS.

Parameter	FF	TT	SS
Input Voltage Range(V)	1.2-1.6	1.2-1.6	1.2-1.6
Iout (mA)	100	100	100
Output Voltage(V)	3.374	3.3714	3.361
Switching Frequency(KHz)	732	724	720
Ripple Voltage(mV)	19	18.29	17.43
Line Regulation(mV/V)	222	235	250
Load Regulation(mV/mA)	9.6	10	10.5
Power Efficiency	97.5	98	98.5

TABLE II
COMPARATIVE ANALYSIS WITH OTHER PUBLISHED PAPERS

Parameter	[3]	[5]	[6]	This work
Input Voltage Range(V)	1.2-1.6	0.8-3	3.3	1.2-1.6
Iout (mA)	100	0-150	14-110	100
Output Voltage(V)	3.3921	3.3	5.8-7	3.3714
Switching Frequency(KHz)	240	-	5500	724
Ripple Voltage(mV)	36.52	-	75	18.29
Line Regulation(mV/V)	237	100	-	235
Load Regulation(mV/mA)	5.48	100	-	10
Power Efficiency	93	95	77	98
Power Dissipation(mW)	348.19	-	300	60.19

Further, the results of the proposed work are compared with [3], [5] and [6] in Table II, it is established that the proposed method gives better performance in terms of reduction in power consumption from 348.19mW [3] to 60.19 mW. The other parameters like the ripple value of the proposed design is 18.29mV whereas in [3] it was 36.52 mV.

CONCLUSION

This paper establishes the design of a highly efficient boost converter generating an output voltage of 3.3 V at load current of 100 mA at a reduced power consumption of 60.19 mV and a low ripple voltage of 18.29 mV for an input range of 1.2 V - 1.6 V. Thus, concluding that the use of Schmitt trigger based ramp generator is more appropriate for designing a boost converter that can be utilized in energy harvesting circuits.

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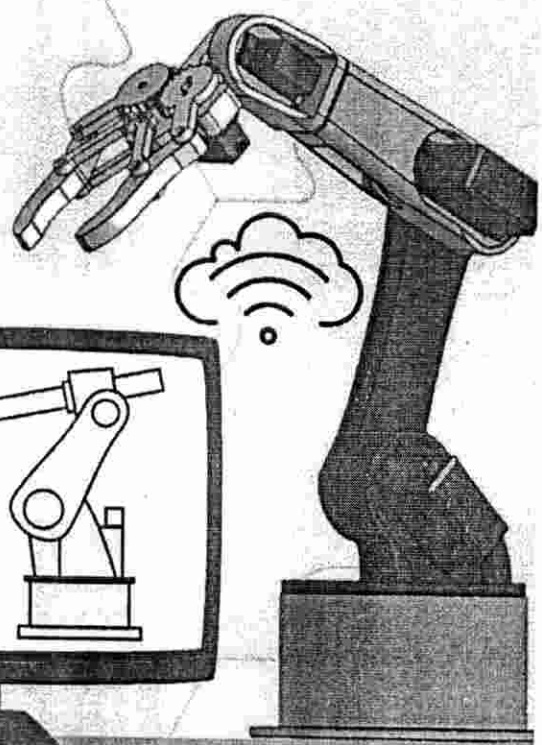

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MUFFAKHAM JAH COLLEGE OF ENGINEERING & TECHNOLOGY
ELECTRONICS AND COMMUNICATION ENGINEERING

Date: 01/12/2020

To

Head of the Department,
Electronics & Communication Engineering Dept,
Muffakham Jah College of Engineering & Technology,
Hyderabad.

Sub: Permission to organize Workshop on "Digital Twin-Robotic Arm"–Reg

Sir,

I am pleased to inform you that a one week workshop on "Digital Twin-Robotic Arm" for the Second Year and Third year Students of E.C.E is scheduled.

Schedule as follows:

Date	**14/12/2020 to 18/12/2020**
Title of Seminar	"Digital Twin-Robotic Arm"
Resource Persons	Dr.Arifuddin Sohel, Mr.Hakeem Aejaz Aslam
Participants	B.E II and III year E.C.E Students

So, I request you to grant the permission to conduct the webinar.

Faculty Incharge

Mr. Hakeem Aejaz Aslam

Assistant Professor, ECED.

30/03/20

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Muffakham Jah College of
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HYDERABAD-500 034.(T.S.)

MUFFAKHAM JAH COLLEGE OF ENGINEERING AND TECHNOLOGY
Department of Electronics and communication Engineering

Date: 05/12/2020

From

Head of the Department,
Electronics & Communication Engineering Dept,
Muffakham Jah College of Engineering & Technology,
Hyderabad.

To
Mr.Hakeem Aejaz Aslam,
Assistant Professor, ECED.

Sub: Conduction of Workshop on "Digital Twin-Robotic Arm"- Regarding.

It is to inform you that the Digital Twin is an emerging technology. There is a need to make students industry ready as per the industry requirements. In this regard, you are requested to design the syllabus and organize a Workshop for the Students of E.C.E on "Digital Twin-Robotic Arm" and inform the date, schedule, resource person and industry/institute.

Thanking You,

Head, ECED

Head of Department
Electronics & Communication Engineering
Muffakham Jah College of Engg. & Tech.
Road No: 3, Banjara Hills Hyderabad-34

30/03/2021
PRINCIPAL
Muffakham Jah College Of Engineering & Technology
Banjara Hills, Road No. 3,
HYDERABAD-500 034.(T.S.)

Date: 05/12/2020

From

Head of the Department,
Electronics & Communication Engineering Dept,
Muffakham Jah College of Engineering & Technology,
Hyderabad.

To
Mr.Hakeem Aejaz Aslam,
Assistant Professor, ECED.

Sub: Conduction of Workshop on "Digital Twin-Robotic Arm"- Regarding.

It is to inform you that the Digital Twin is an emerging technology. There is a need to make students industry ready as per the industry requirements. In this regard, you are requested to plan a Workshop for the Students of E.C.E on "Digital Twin-Robotic Arm" and inform the date, schedule, resource person and industry/institute.

Thanking You,

Head, ECED

Head
Electronics & Communication Engineering
Muffakham Jah College of Engg. & Tech.
Road No: 3, Banjara Hills Hyderabad-34

3-12-03/2020

PRINCIPAL
Muffakham Jah College of
Engineering & Technology
Banjara Hills, Road No. 3,
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Minutes of Meeting

Date: 05/12/2020 **Venue:** HOD Room Time: 10:00AM to 11:00AM

Agenda: "Digital Twin-Robotic Arm" regarding:

This meeting was conducted in offline mode regarding the Digital Twin-Robotic Arm which is to be organized in the college from 14th Dec, 2020 to 18th Dec, 2020.

Chairperson: 1. Dr. Arifuddin Sohel, Head of ECE Dept.
2. Mr.Hakeem Aejaz Aslam, Assistant Professor and Coordinator

For the workshop the following things were discussed:

1. Session will start from 9am to 4pm for one week.
2. Last date to register for the workshop is 10th Dec, 2020.
3. Main focus on 2nd & 3rd year students.
4. All the datasets and software should share with participants.
5. Attendance is mandatory to issue the participation of certificate.
6. At the end of the workshop, participants will be required to submit the feedback regarding the workshop.

Attendees:

1. Dr. Arifuddin Sohel
2. Mr.Hakeem Aejaz Aslam
3. Mr. Abdul Khader (Student Representative)
4. Anas(Student Representative)

Prepared By,

Mr. Hakeem Aejaz Aslam, Asst. Prof., ECE dept

30/03/2021

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Muffakham Jah College Of
Engineering & Technology
Banjara Hills, Road No. 3,
HYDERABAD-500 034.(T.S.)

Dr. Arifuddin Sohel,

Head of ECE Dept.

FEEDBACK ANALYSIS OF WORKSHOP ON "DIGITAL TWIN-ROBOTIC ARM"

S.No	Mail id	Name	Roll Number	1	2	3	4	5	6	7	8
1	fareha.fatima01@gmail.com	Fareha Fatima	1604-15-735-009	yes	5	5	5	5	5	5	5
2	160416735023@mjcollege.ac.in	Mohammed Ashfaq Hussain	1604-16-735-023	yes	5	5	4	5	5	5	4
3	160417735094@mjcollege.ac.in	Sameer Hasnain Maarif	1604-17-735-094	yes	5	4	2	5	4	5	2
4	160418735001@mjcollege.ac.in	Ayeman Fatima	1604-18-735-001	yes	5	5	5	5	5	5	5
5	160418735002@mjcollege.ac.in	Nida	1604-18-735-002	yes	5	5	5	5	5	4	5
6	160418735003@mjcollege.ac.in	Asfiya Jabeen	1604-18-735-003	yes	5	5	5	5	5	5	5
7	160418735004@mjcollege.ac.in	Firdous Fathima	1604-18-735-004	yes	4	5	4	5	5	5	4
8	160418735007@mjcollege.ac.in	syeda mehvish anwar	1604-18-735-007	yes	5	5	5	5	5	5	5
9	160418735008@mjcollege.ac.in	Asma Siddiqua	1604-18-735-008	yes	5	4	5	5	5	5	5
10	160418735009@mjcollege.ac.in	Fareha Fatima	1604-18-735-009	yes	5	5	5	5	4	5	5
11	160418735010@mjcollege.ac.in	Tahereen Rizvi	1604-18-735-010	yes	5	5	5	5	5	4	5
12	160418735011@mjcollege.ac.in	N AMAN ARMAN KHAN	1604-18-735-011	yes	4	5	5	5	5	5	5
13	160418735014@mjcollege.ac.in	M.A.RAZAQ KHAN	1604-18-735-014	yes	5	5	4	5	5	3	4
14	160418735016@mjcollege.ac.in	Bilal Adnan	1604-18-735-016	yes	5	3	5	5	5	5	5
15	160418735017@mjcollege.ac.in	Mohammad Ibrahim	1604-18-735-017	yes	5	5	5	4	5	5	5
16	160418735021@mjcollege.ac.in	Syed Diraar Ahmed	1604-18-735-021	yes	4	5	5	5	5	4	5
17	160418735023@mjcollege.ac.in	Syed shoaib ali	1604-18-735-023	yes	5	5	5	5	5	5	5
18	160418735029@mjcollege.ac.in	Mohammad Asif Ahmed	1604-18-735-029	yes	3	4	5	5	5	5	5
19	160418735032@mjcollege.ac.in	Mohd Adil Ahmed	1604-18-735-032	yes	5	5	5	5	4	5	5
20	160418735032@mjcollege.ac.in	Mohd Adil Ahmed	1604-18-735-032	yes	4	5	5	3	5	4	5
21	160418735033@mjcollege.ac.in	Mujtabauddin Ahmed	1604-18-735-033	yes	5	5	4	5	5	5	4
22	160418735034@mjcollege.ac.in	Md Ibrahim	1604-18-735-034	yes	5	5	5	5	5	5	5
23	160418735036@mjcollege.ac.in	Mohammad Adil Parwez	1604-18-735-036	yes	5	4	5	3	5	5	5
24	160418735038@mjcollege.ac.in	SHAIK ABU ANZAR SAYEED	1604-18-735-038	yes	5	5	5	5	5	3	5
25	160418735039@mjcollege.ac.in	Mohammed rafeeq khan	1604-18-735-039	yes	4	3	5	4	5	5	5
26	160418735040@mjcollege.ac.in	Syed Saquib Ahmed	1604-18-735-040	yes	5	5	5	5	4	4	5
27	160418735041@mjcollege.ac.in	Syed Ayaan Ahmed	1604-18-735-041	yes	4	5	5	5	5	5	5
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29	160418735057@mjcollege.ac.in	Syed osman shareef	1604-18-735-057	yes	5	5	5	4	5	5	5
30	160418735063@mjcollege.ac.in	Bushra shereen	1604-18-735-063	yes	3	5	5	5	4	4	5
31	160418735065@mjcollege.ac.in	R Shahina sultana	1604-18-735-065	yes	5	5	4	5	5	5	4
32	160418735068@mjcollege.ac.in	safia wajeed •	1604-18-735-068	yes	3	5	5	5	5	5	5
33	160418735071@mjcollege.ac.in	Aakanksha Thodupunoori	1604-18-735-071	yes	4	5	5	4	5	3	5
34	160418735072@mjcollege.ac.in	Sai Rithvik Gundla	1604-18-735-072	yes	5	5	5	5	5	5	5
35	160418735075@mjcollege.ac.in	koushik	1604-18-735-075	yes	5	5	5	5	4	5	5
36	160418735076@mjcollege.ac.in	Ch.Harsha Vardhan	1604-18-735-076	yes	5	5	5	5	5	5	5
37	160418735077@mjcollege.ac.in	Syed Ali Hyder	1604-18-735-077	yes	5	5	5	5	5	5	5
38	160418735079@mjcollege.ac.in	Mohammad Riaz	1604-18-735-079	yes	5	5	5	5	5	5	5
39	160418735080@mjcollege.ac.in	Anvith	1604-18-735-080	yes	5	5	5	5	5	4	5
40	160418735081@mjcollege.ac.in	Hamza Shah Khan	1604-18-735-081	yes	5	5	3	5	3	5	3
41	160418735084@mjcollege.ac.in	MOHAMMED AKBAR	1604-18-735-084	yes	5	5	5	5	4	5	5
42	160418735086@mjcollege.ac.in	sai mohith chinnari	1604-18-735-086	yes	5	3	4	4	5	5	4
43	160418735089@mjcollege.ac.in	Khaja Mohammad Faizuddin	1604-18-735-089	yes	5	5	5	5	5	5	5
44	160418735093@mjcollege.ac.in	Syed Muzammil	1604-18-735-093	yes	5	5	5	5	5	5	5
45	160418735094@mjcollege.ac.in	shoaib	1604-18-735-094	NO	5	5	4	5	5	5	4
46	160418735095@mjcollege.ac.in	Shaik seif shah	1604-18-735-095	yes	5	5	5	5	5	5	5
47	160418735097@mjcollege.ac.in	MOHAMMED ASIM SIDDIQUI	1604-18-735-097	yes	5	5	5	5	5	5	5
48	160418735118@mjcollege.ac.in	MOHAMMED WAJAHAT HUSSAIN	1604-18-735-118	yes	5	3	5	5	5	4	5
49	160418735119@mjcollege.ac.in	Mohammed abdur Rahman	1604-18-735-119	yes	5	5	5	5	5	5	5
50	160418735303@mjcollege.ac.in	MOHAMMED ABDUL HAMEED	1604-18-735-303	yes	5	5	5	5	5	5	5
51	160418735304@mjcollege.ac.in	Abdul Samad Khan	1604-18-735-304	yes	5	5	5	5	5	5	5
52	160418735305@mjcollege.ac.in	Shaik sahera begum	1604-18-735-305	yes	5	5	5	5	5	5	5
53	160418735308@mjcollege.ac.in	Mohammed Abdullah Rizwan	1604-18-735-308	yes	5	5	5	5	5	5	5
54	160418735310@mjcollege.ac.in	Hafsa Maryam	1604-18-735-310	yes	5	5	5	5	5	4	5
55	160418735311@mjcollege.ac.in	Shaik Musharraf ali	1604-18-735-311	yes	5	5	5	5	5	5	5
56	160418735312@mjcollege.ac.in	Mohammed Salman Khan	1604-18-735-312	yes	5	5	5	5	5	3	5

Feebback Question

1. It was excellent
2. The workshop met your Expectations
3. Your level of knowledge at the start of the workshop
4. How satisfied were you with the session content?
5. The tutor was open to new ideas and view points
6. The tutor took account of students existing knowledge and level of understanding
7. Adequacy of slides in terms of coverage of workshop
8. Precision and answering the questions by the tutor

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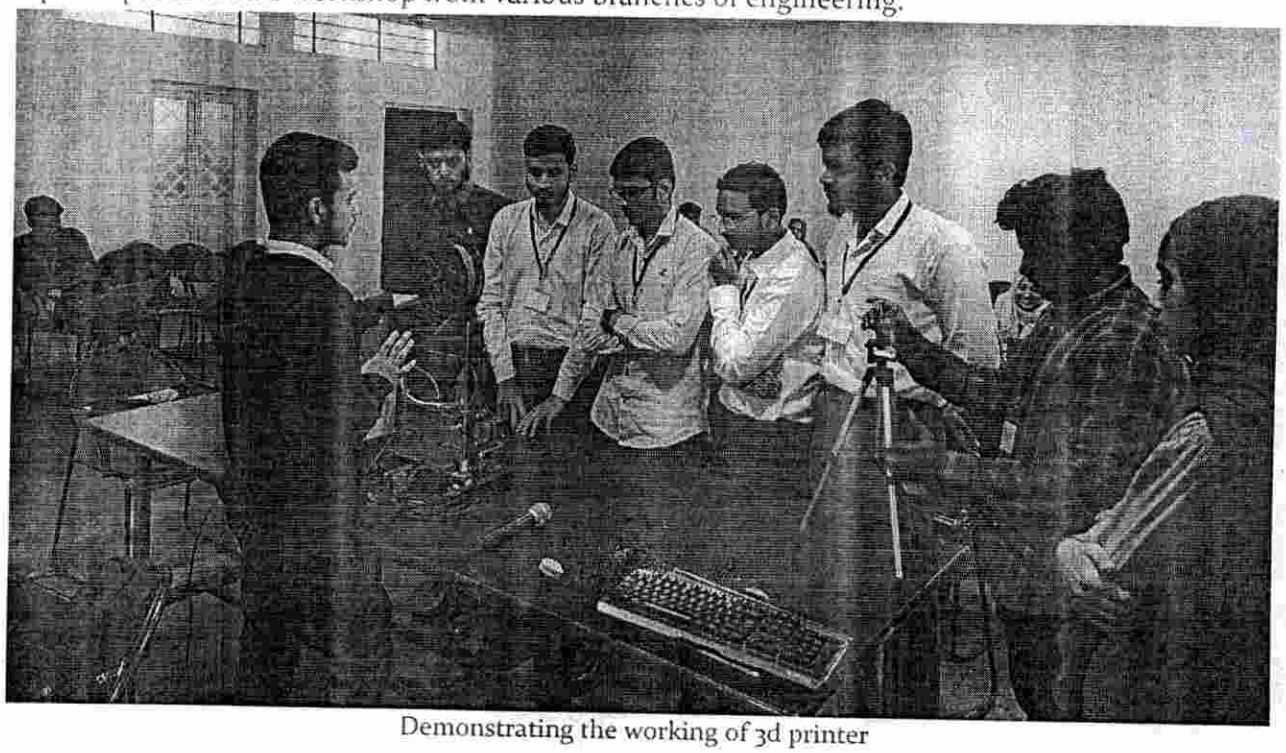
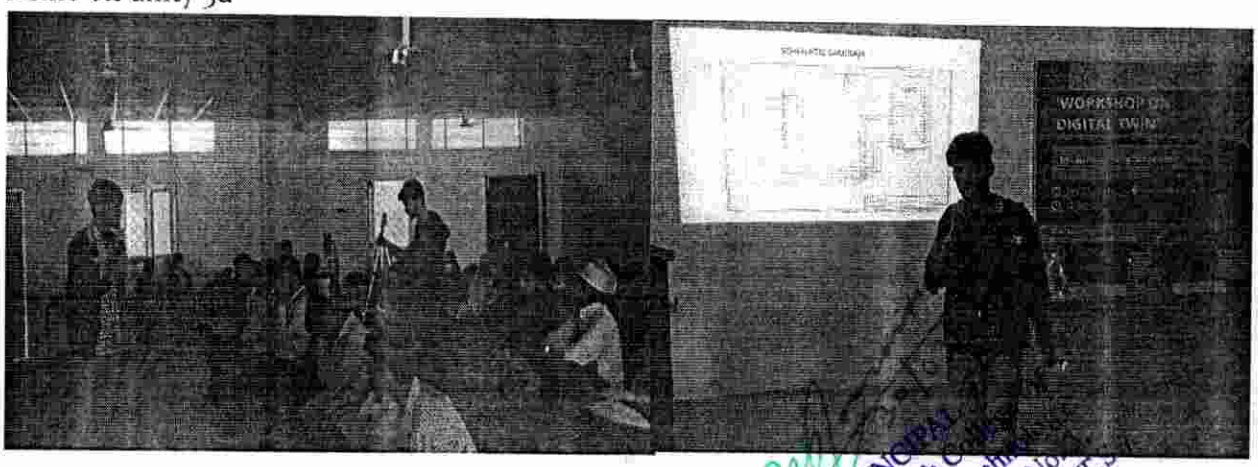
Dr. Mohammed Arifuddin Sohel, Secretory IEEE Hyderabad section, Chair RAS Chapter, Head ECED, MJCET and also the workshop coordinator presented the talk on digital twin technology and introduced to the digital twin and robotic arm and the importance and applications/uses of it and informed the gathering that the workshop is being organized to spread the knowledge of digital twin technology and robotic arm to the various engineering students from both rural and urban areas. All most thirty students were participated in this workshop from various branches of engineering.



Demonstrating the working of 3d printer

The following things was discussed and demonstrated in the session...

- Introduction to digital twin
- Overview of robotic arm
- Onshape CAD modelling
- Node MCU & Servo introduction
- Introduced to easyeda & schematic structure
- Arduino programing
- Demonstration to BLYNK application
- Demo on unity 3d

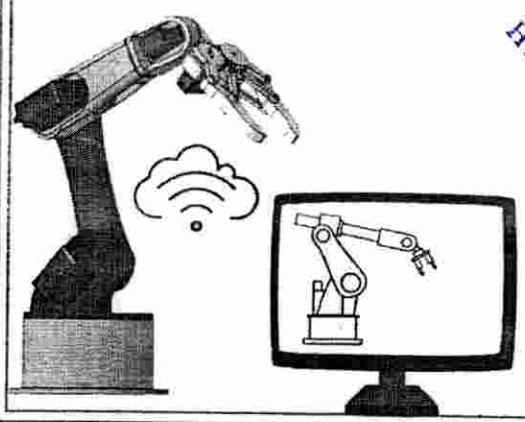


CERTIFICATE OF PARTICIPATION

This certificate is proudly presented to

IEEE

For participating in the "Digital Twin" Workshop on December 14th & 18th, 2020.



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Dr. Arifuddin Sohel
Secretary
IEEE Hyderabad Section.
Head ECE Dept,MJCET.

Outcome of the workshop "Digital Twin-Robotic Arm"

Many students have done mini projects and hardware models based on the knowledge what they have gained from this one week workshop: Digital Twin-Robotic Arm.

1. To make use of open source tools like Solidworks CAD for designing
2. Use of 3D printer for making the bots
3. Writing the codes & simulating them
4. Debugging the software codes
5. Assembling the hardware parts etc.

30/03/2022

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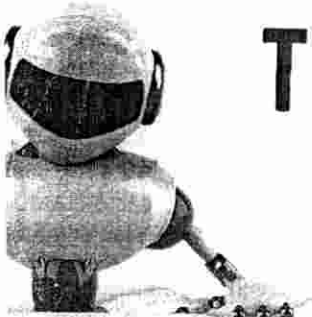
MUFFAKHAM JAH
COLLEGE OF ENGINEERING AND TECHNOLOGY.

CAS
IEEE CIRCUITS AND SYSTEMS SOCIETY

NAT



T-SIGNATURE MJCET & IEEE CAS

PRESENTS...

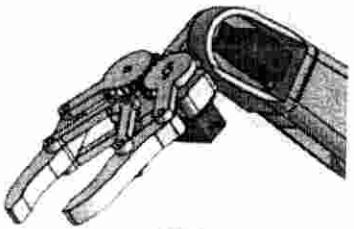
HOP ON...

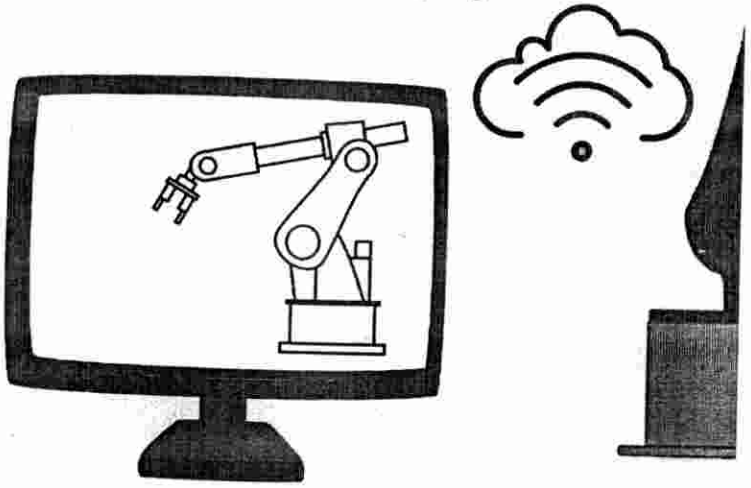
DIGITAL TWIN!

ECEMBER 14TH TO 18TH 2020

00-4:00 PM

UDENT ACTIVITY CENTER





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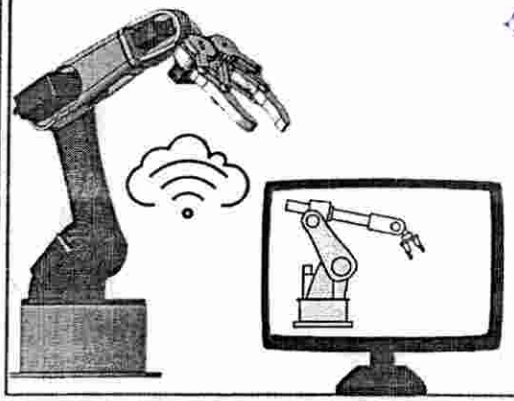
Juweriya

For participating in the "Digital Twin" Workshop on December 14th To 18th, 2020.



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20/03/2021

Dr. Arifuddin Sohel
Secretary
IEEE Hyderabad Section.
Head ECE Dept,MJCET.

CERTIFICATE OF PARTICIPATION

This certificate is proudly presented to

Maaz Khan

For participating in the "Digital Twin" Workshop on December 14th To 18th, 2020.

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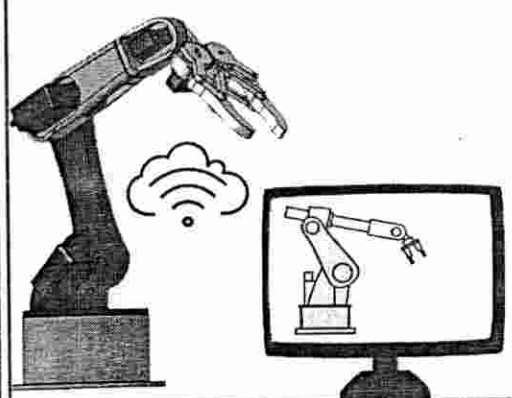


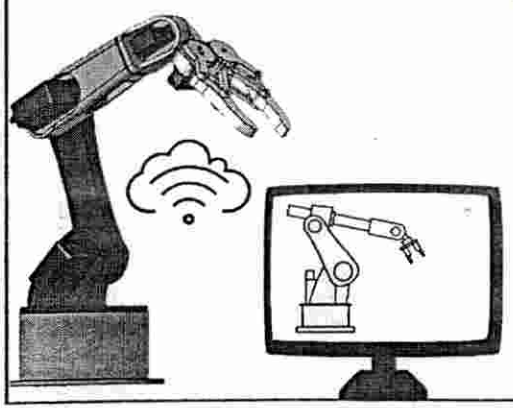
Dr. Arifuddin Sohel
Secretary
IEEE Hyderabad Section.
Head ECE Dept,MJCET.

CERTIFICATE OF PARTICIPATION

This certificate is proudly presented to

Qurram Ali Ibad

For participating in the "Digital Twin" Workshop on December 14th To 18th, 2020.



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Maulana Azad National Urdu University
Engineering & Technology
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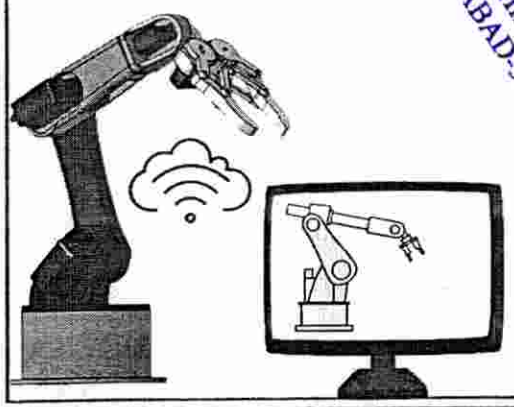
Dr. Arifuddin Sohel
Secretary
IEEE Hyderabad Section.
Head ECE Dept,MJCET.

CERTIFICATE OF PARTICIPATION

This certificate is proudly presented to

Abdullah Khan

For participating in the "Digital Twin" Workshop on December 14th To 18th, 2020.



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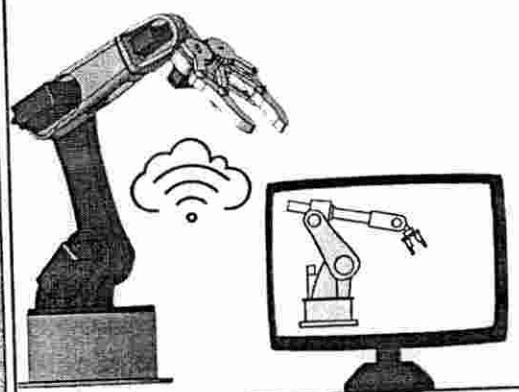
Dr. Arifuddin Sohel
Secretary
IEEE Hyderabad Section.
Head ECE Dept,MJCET.

CERTIFICATE OF PARTICIPATION

This certificate is proudly presented to

Syed Saffan Ahmed

For participating in the "Digital Twin" Workshop on December 14th To 18th, 2020.



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Dr. Arifuddin Sohel
Secretary
IEEE Hyderabad Section.
Head ECE Dept,MJCET.

Institute of Electrical and Electronics Engineers (IEEE)
Hyderabad Section

Hyderabad Secti

1 Signature of Certificate

Special Interest Group (SiG) on IoT, IEEE Hyderabad Section

A unit of Joint Chapter of Circuits and Systems and Electron Devices (CAS/ED) Societies

5 Sample Certificate

In collaboration with

Electronics and Communication Engineering Department
Muffakham Jah College of Engineering and Technology, Hyderabad

Presents

Two weeks workshop on

Internet of Things (IoT)

6th Feb-14 Feb 2021

[illegible] Technology of Internet of things is taking rapid strides in the connected world and with implementation of 5G network this technology will become the most heavily used technology of the century. With this in the main objective of the workshop is to train the faculty and PG students on practical experiments in IoT lab. The IEEE Hyde section has recently established a Verification and Validation lab in ECE Department of MJCET which serves as a model pol of continuous testing of the IEEE standard 1451.99. The main aim of this workshop is to provide technical guidance abo process of establishment of an IoT lab, components and equipment's required to do the setup, provision of LAB manual/ experiments based on Node MCU and Raspberry Pi and finally to present the Bill of materials for financial estimation to set up in all engineering colleges with technical support from IEEE Hyderabad section.

Workshop Faculty:

Dr. Mohammad Arif Sobel is having 15 years of teaching experience in the field of VLSI Designs currently champions cause of spreading [illegible] in the area of Internet of Things(IoT). He has conducted many workshops on the topics of [illegible] and systems. He is instrumental in the setup of Verifi [illegible] standards. Arif Sobel is cur [illegible] chapter of Hyderabad Sectio

Workshop Schedule and Topics:

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MUFFAKHAM JAH COLLEGE OF ENGINEERING & TECHNOLOGY
ELECTRONICS AND COMMUNICATION ENGINEERING

Date: 21/1/2021

To

Head of the Department,
Electronics & Communication Engineering Dept,
Muffakham Jah College of Engineering & Technology,
Hyderabad.

Sub: Permission to organize Workshop on "Internet of Things" –Reg

Sir,

I am pleased to inform you that a 2 Week Workshop on "Internet of Things" for the First Year Students of E.C.E is scheduled.

Schedule as follows

Date	6/2/21,7/2/21 13/2/21,14/2/21
Title of Seminar	" Internet of Things"
Resource Persons	Dr.Arifuddin sohel, Mr.Noorullah khan
Participants	B.E I year E.C.E Students

So, I request you to grant the permission to conduct the workshop.

Faculty In charge

Mohammed Muneeruddin,

Sr.Asst.Professor

30/03/2021

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MUFFAKHAM JAH COLLEGE OF ENGINEERING & TECHNOLOGY
ELECTRONICS AND COMMUNICATION ENGINEERING

Date: 18/01/2021

To
Mohammed Muneeruddin
Sr.Asst.Professor

Sub: Conduction of Workshop on "Internet of Things"- Regarding.

It is to inform you that the Internet of Things is an emerging technology. Students must be industry ready as per the industry requirements. In this regard, you are requested to plan a Workshop for the Students of E.C.E on "Internet of Things" and inform the date, schedule, resource person and industry/institute.

Thanking You,

Head,ECED

Head of Department
Electronics & Communication Engineering
Muffakham Jah College of Engg. & Tech.
Road No: 3, Banjara Hills Hyderabad-34

24/03/2021
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Minutes of Meeting

Date: 19/01/2021 **Venue:** offline mode Time: 10:00AM to 11:00AM

Agenda: workshop on Internet of Things -reg

This meeting was conducted in offline mode regarding the Internet of things which is to be organized in the college from 6, 7, 13, 14 Feb, 2021.

Chairperson: 1 .Dr. Mohammed Arifuddin Sohel, Head of ECE Dept.
2. Mr. Muneeruddin, Coordinator

For the workshop the following things were discussed.

1. Session will start from 6/2/21
2. Last date to register for the workshop is 4 Feb,2021.
3. Focus on First year students.
4. All the datasets and software should share with participants.
5. Attendance is mandatory to issue the participation of certificate
6. At the end of the workshop, participants will be required to submit a mini project based knowledge what they gain from workshop.

Attendees:

1. Mr. M A RAHEEM
2. MR Noorullah khan
3. Taha (Student Representative)
4. Amaan (Student Representative)
5. Mehvish (Student Representative)

Prepared By,

Mr. Muneeruddin, Sr. Asst. Prof., ECE dept

Dr. Mohammed Arifuddin Sohel,

Head of ECE Dept

30/01/2021

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Muffakham Jah College of Engineering and Technology

(THE SULTAN UL ULOOM EDUCATION SOCIETY) Affiliated to Osmania University &
Recognized by AICTE Banjara Hills, Hyderabad - 500 034

2 Week Workshop

on

Internet of Things

by

ECED,MJCET,HYDERABAD

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Banjara Hills, Road No. 3
HYDERABAD-500034 (T.S.)

Speakers:

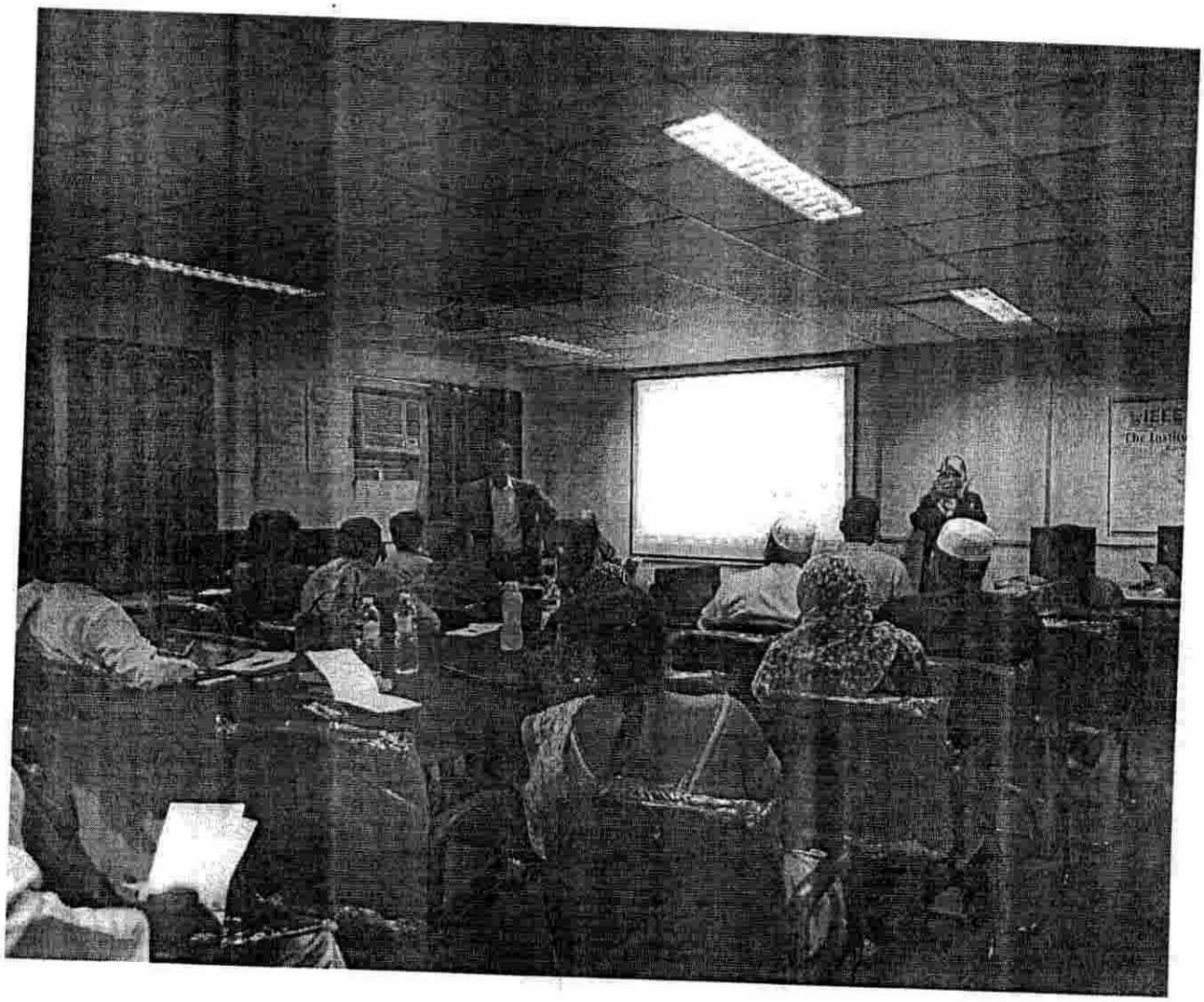
1. **Dr. Arifuddin Sohel**
2. **Mr.Mohammed Muneeruddin**
3. **Mr.Noorullah**

Duration : 6 Feb,2021 to 14th Feb ,2021(9am to 5pm)

Workshop

on

Internet of Things



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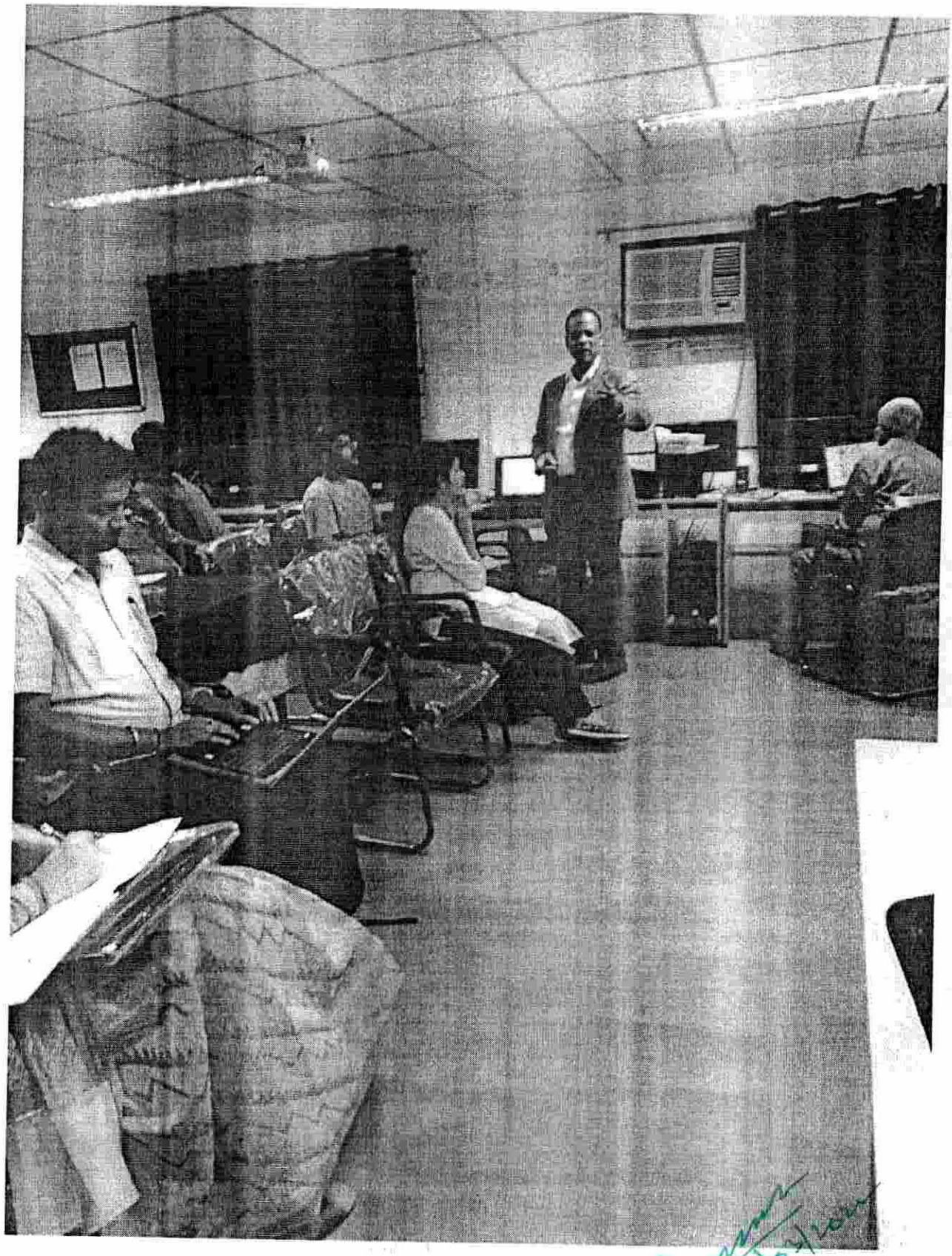

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Workshop on Internet of things

S.No	Email id		6th feb	7th feb	13th feb	14th feb
1	1604-20-735-001@mjcollege.ac.in		present	present	present	present
2	1604-20-735-002@mjcollege.ac.in	Saniya Begum	present	present	present	present
3	1604-20-735-003@micollege.ac.in	Diya Agarwal	present	present	present	Absent
4	1604-20-735-004@mjcollege.ac.in	Sanya Begum	present	present	present	present
5	1604-20-735-005@mjcollege.ac.in	Sabahat Maheen	present	Absent	present	present
6	1604-20-735-006@mjcollege.ac.in	Alla Swapnika Sri	present	present	present	present
7	1604-20-735-007@mjcollege.ac.in	Naziya Anjum	present	present	present	present
8	1604-20-735-008@micollege.ac.in	Nimra Ali Siddiqui	present	present	present	present
9	1604-20-735-009@mjcollege.ac.in	Sarah Firdious	Absent	Absent	present	Absent
10	1604-20-735-010@micollege.ac.in@mjcollege.ac.in	Rabiya Mohammadi Syeda	present	present	present	present
11	1604-20-735-011@mjcollege.ac.in	Ayesha Midhath Anam	present	present	Absent	present
12	1604-20-735-012@micollege.ac.in	Shaishta Daniya	present	present	present	present
13	1604-20-735-013@mjcollege.ac.in	Hafsa Jaziba	present	present	present	present
14	1604-20-735-014@mjcollege.ac.in	Syeda Huzaifah Younus	present	present	present	present
15	1604-20-735-015@mjcollege.ac.in	Nandyala Kalam Basha	present	present	present	present
16	1604-20-735-016@micollege.ac.in	Mohammed Emad Sultan Siddiqi	present	present	present	present
17	1604-20-735-017@mjcollege.ac.in	Md Wajahath	present	present	present	present
18	1604-20-735-018@mjcollege.ac.in	Mahmood Khan	present	Absent	present	present
19	1604-20-735-019@mjcollege.ac.in	Mohamed Nawaz Ahmed	present	present	Absent	present
20	1604-20-735-020@micollege.ac.in	Syed Saffan Ahmed	present	present	present	present
21	1604-20-735-021@micollege.ac.in	Thowheedulla Khan	Absent	present	present	Absent
22	1604-20-735-022@mjcollege.ac.in	Mohammed Mohtasimuddin	present	present	present	present
23	1604-20-735-023@mjcollege.ac.in	Waheed Khan	present	present	present	present
24	1604-20-735-024@mjcollege.ac.in	Gore Mohammed Farhan ullah	present	present	present	present
25	1604-20-735-025@mjcollege.ac.in	Mohammed Amaan Ali	present	present	present	present
26	1604-20-735-029@mjcollege.ac.in	Mohammad Arbaz	present	present	present	present
27	1604-20-735-030@mjcollege.ac.in	Mohammed Anas Mahboob Ali	present	present	Absent	present
28	1604-20-735-031@mjcollege.ac.in	Syed Khaif Mohiuddin	present	present	present	present
29	1604-20-735-032@mjcollege.ac.in	Arshad Ahmed Shareef	present	present	present	Absent
30	1604-20-735-033@mjcollege.ac.in	Rehan Ahmed	present	present	present	present
31	1604-20-735-034@mjcollege.ac.in	Mohammed Shahid Ali	present	Absent	present	present
32	1604-20-735-035@mjcollege.ac.in	Mohammed Zubair	present	present	present	present
33	1604-20-735-036@micollege.ac.in	Mohammed Mustafa Abrar	present	present	present	present
34	1604-20-735-037@mjcollege.ac.in	Syed Danish Amaan	present	present	present	present
35	1604-20-735-038@mjcollege.ac.in	Mohammed Saif ur Rahman	Absent	present	present	present
36	1604-20-735-039@mjcollege.ac.in	Md Mahboob Zeeshan	present	present	present	Absent
37	1604-20-735-040@mjcollege.ac.in	Mohammed Haneef	present	present	present	present
38	1604-20-735-041@mjcollege.ac.in	Mohd Bilal Ahmed	present	present	present	present
39	1604-20-735-042@mjcollege.ac.in	Mohammed Bin Omer	present	present	present	present
40	1604-20-735-043@micollege.ac.in	Mohammed Aathif Junaid	present	present	Absent	Absent
41	1604-20-735-046@mjcollege.ac.in	Safwan Mohammed	present	present	present	present
42	1604-20-735-047@mjcollege.ac.in	Mohammed Bilal Ahmed	present	present	present	present
43	1604-20-735-048@mjcollege.ac.in	Mir Ahmed Ali	Absent	present	present	present
44	1604-20-735-049@mjcollege.ac.in	Syed Salluddin	present	present	present	present
45	1604-20-735-050@mjcollege.ac.in	Mohamed Akhtar	present	present	present	present
46	1604-20-735-051@mjcollege.ac.in	Fahat Bar Khan	present	present	present	present
47	1604-20-735-052@mjcollege.ac.in	Mohd Hamza Anwar	present	present	present	present
48	1604-20-735-053@mjcollege.ac.in	Mohammed Maaz Waheed	present	present	present	Absent
49	1604-20-735-054@mjcollege.ac.in	Syed Anas Mannan Ahmed	present	present	present	present
50	1604-20-735-056@mjcollege.ac.in	Mohammed Farooq				

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51	1604-20-735-057@mjcollege.ac.in	Syed Ibrahim uddin	Absent	present	present	present
52	1604-20-735-058@mjcollege.ac.in	Syed Yahiya	present	present	Absent	present
53	1604-20-735-059@mjcollege.ac.in	Mohd Ghouse Tazeem	present	present	present	present
54	1604-20-735-060@mjcollege.ac.in	Syed Rayanuddin	present	present	present	Absent
55	1604-20-735-061@mjcollege.ac.in	Mir Hasan Ali Abedi	present	present	present	present
56	1604-20-735-062@mjcollege.ac.in	Aiman Jameel	present	present	Absent	present
57	1604-20-735-063@mjcollege.ac.in	Saniya Khanam	present	present	present	present
58	1604-20-735-064@mjcollege.ac.in	Fouziyah Shirin	present	present	present	present
59	1604-20-735-065@mjcollege.ac.in	Sameeha Hameed	present	present	present	Absent
60	1604-20-735-066@mjcollege.ac.in	Zeba	present	present	present	present
61	1604-20-735-067@mjcollege.ac.in	Anees unnisa	present	Absent	present	present
62	1604-20-735-068@mjcollege.ac.in	Maleeha Naba	present	present	present	present
63	1604-20-735-069@mjcollege.ac.in	Hurmath Sara	present	present	present	present
64	1604-20-735-070@mjcollege.ac.in	Zainab Sultana	present	present	present	present
65	1604-20-735-071@mjcollege.ac.in	Zaid Amer Syed	Absent	Absent	present	Absent
66	1604-20-735-072@mjcollege.ac.in	Ayyub Khan	present	present	present	present
67	1604-20-735-074@mjcollege.ac.in	Md Furqan Hasan	present	present	Absent	present
68	1604-20-735-075@mjcollege.ac.in	Ahsan Baseer	present	present	present	present
69	1604-20-735-076@mjcollege.ac.in	Mohammed Sufyan Saleem	present	present	present	present
70	1604-20-735-077@mjcollege.ac.in	Mohammed Ilyas Ahmed	present	present	present	present
71	1604-20-735-078@mjcollege.ac.in	Syed Rehan Malik	present	present	present	present
72	1604-20-735-079@mjcollege.ac.in	Hasan Ali Al Qattan	present	present	present	present
73	1604-20-735-081@mjcollege.ac.in	Mohammed Nabeel	present	present	present	present
74	1604-20-735-082@mjcollege.ac.in	Quazi Zainuddin Ahmed Siddiqui	present	Absent	present	present
75	1604-20-735-083@mjcollege.ac.in	Faraaz Siddiqui	present	present	Absent	present
76	1604-20-735-084@mjcollege.ac.in	Shaik Fayaz Ahmed	present	present	present	present
77	1604-20-735-085@mjcollege.ac.in	Mohammed Irfan Khan	Absent	present	present	Absent
78	1604-20-735-086@mjcollege.ac.in	Syed Khaja Fakhruddin	present	present	present	present
79	1604-20-735-087@mjcollege.ac.in	Mohammed Faizan Ahmed	present	present	present	present
80	1604-20-735-088@mjcollege.ac.in	Omer Farooq	present	present	present	present
81	1604-20-735-090@mjcollege.ac.in	Ghulam Ahmed Ibraaz Mohiuddin	present	present	present	present
82	1604-20-735-091@mjcollege.ac.in	Mohammed Faizan Shah	present	present	present	present
83	1604-20-735-092@mjcollege.ac.in	Mohammed Hassan Ahmed	present	present	Absent	present
84	1604-20-735-093@mjcollege.ac.in	Mohammed Salahuddin	present	present	present	present
85	1604-20-735-094@mjcollege.ac.in	Mohd Gufran Khursheed	present	present	present	Absent
86	1604-20-735-095@mjcollege.ac.in	Mohd Mehraj Ahmed	present	present	present	present
87	1604-20-735-096@mjcollege.ac.in	Mohammed Sami uddin	present	Absent	present	present
88	1604-20-735-097@mjcollege.ac.in	Syed Imtiyaz Ali	present	present	present	present
89	1604-20-735-098@mjcollege.ac.in	Anzar Irfan Khan	present	present	present	present
90	1604-20-735-099@mjcollege.ac.in	Sk Khadir Pasha	present	present	present	present
91	1604-20-735-100@mjcollege.ac.in	Mohd Zahed Khan	Absent	present	present	present
92	1604-20-735-101@mjcollege.ac.in	Hamzah Habeeb Iqbal	present	present	present	Absent
93	1604-20-735-102@mjcollege.ac.in	Mirza Sameeullah Baig	present	present	present	present
94	1604-20-735-103@mjcollege.ac.in	Huzaifa Abdul Wadood Siddiqui	present	present	present	present
95	1604-20-735-104@mjcollege.ac.in	Farhan Ahmed	present	present	present	present
96	1604-20-735-105@mjcollege.ac.in	Syed Arhhann Ahmad	present	present	Absent	Absent
97	1604-20-735-106@mjcollege.ac.in	Mohammed Amaan Ali	present	present	present	present
98	1604-20-735-110@mjcollege.ac.in	Syed Haseeb uddin	present	present	present	present
99	1604-20-735-111@mjcollege.ac.in	Shaik Irshad Ahmed	present	present	present	present
100	1604-20-735-112@mjcollege.ac.in	Mohammad Abdul Arshad	present	present	present	present
101	1604-20-735-113@mjcollege.ac.in	Abdul Quadir Omer	present	present	present	present
102	1604-20-735-114@mjcollege.ac.in	Mohd Abdullah Sobaan	present	present	present	present
103	1604-20-735-115@mjcollege.ac.in	Abdullah Khan	present	present	present	present

104	1604-20-735-116@mjcollege.ac.in	***Mohd Mirza Asgar Hadi***	present	present	present	Absent
105	1604-20-735-117@mjcollege.ac.in	***Mohammed Adnan***	present	present	present	present
106	1604-20-735-118@mjcollege.ac.in	***Mohd Adnan Pasha***	present	present	present	present
107	1604-20-735-119@mjcollege.ac.in	***Syed Ahmed Khasim Ghouri***	Absent	present	present	present
108	1604-20-735-120@mjcollege.ac.in	***Makhan Vishal Singh***	present	present	Absent	present
		Syed Nawaz				

30/03/2022

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Certificate of Achievement

Muffakhamjah college of Engineering and Technology

This certificate is presented to

for attending the Workshop "Internet of things " organized by the Department of Electronics and communication, MJCET from 6 Feb to 14th Feb 21.

Dr.Arifuddin sohel
Head ECED

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HYDERABAD-500 034.(T.S.)

Internet of Things workshop

Feedback Form

Thank you for participating in our event. We hope you had as much fun attending as we did organizing it.

We want to hear your feedback so we can keep improving our logistics and content. Please fill this quick survey and let us know your thoughts (your answers will be anonymous).

1. It was excellent

Yes No

Participant Up gradation

1. The workshop met your Expectations

	1	2	3	4	5	
Poor	○	○	○	○	○	Excellent

1. Your level of knowledge at the start of the workshop

	1	2	3	4	5	
Poor	○	○	○	○	○	Excellent

1. How satisfied were you with the session content?

	1	2	3	4	5	
Poor	○	○	○	○	○	Excellent

30/05/2018

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Banjara Hills, Road No. 3,
HYDERABAD-500 034.(T.S.)

Tutor Involvement

1. The tutor was open to new ideas and view points

	1	2	3	4	5	
Poor	○	○	○	○	○	Excellent

1. The tutor took account of students existing knowledge and level of understanding

	1	2	3	4	5	
Poor	○	○	○	○	○	Excellent

1. Adequacy of slides in terms of coverage of workshop

	1	2	3	4	5	
Poor	○	○	○	○	○	Excellent

1. Precision and answering the questions by the tutor

	1	2	3	4	5	
Poor	○	○	○	○	○	Excellent

30/9/21

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HYDERABAD-500 034.(T.S.)

INTERNET OF THINGS FEEDBACK ANALYSIS

No	Mail id	Mail id	Roll Numbe	1	2	3	4	5	6	7	8
1	1604-20-735-001@mjcollege.ac.in	*Saniya Begum*	*1604-20-735-001*	yes	4	5	5	4	5	3	5
2	1604-20-735-002@mjcollege.ac.in	*Diya Agarwal*	*1604-20-735-002*	yes	5	5	5	5	5	5	5
3	1604-20-735-003@mjcollege.ac.in	*Sanya Begum*	*1604-20-735-003*	yes	5	5	5	5	4	5	5
4	1604-20-735-004@mjcollege.ac.in	*Sabahat Maheen*	*1604-20-735-004*	yes	5	5	5	5	5	5	5
5	1604-20-735-005@mjcollege.ac.in	*Alla Swapnika Sri*	*1604-20-735-005*	yes	5	5	5	5	5	5	5
6	1604-20-735-006@mjcollege.ac.in	*Naziya Anjum*	*1604-20-735-006*	yes	5	5	5	5	5	5	5
7	1604-20-735-007@mjcollege.ac.in	*Nimra Ali Siddiqui*	*1604-20-735-007*	yes	5	5	5	5	4	5	5
8	1604-20-735-008@mjcollege.ac.in	*Sarah Firdious*	*1604-20-735-008*	yes	4	5	5	3	5	4	5
9	1604-20-735-009@mjcollege.ac.in	*Rabiya Mohammadi Syeda*	*1604-20-735-009*	yes	5	5	4	5	5	5	4
10	1604-20-735-010@mjcollege.ac.in@mjcollege.ac.in	*Ayesha Midhath Anam*	*1604-20-735-010*	yes	5	5	5	5	4	5	5
11	1604-20-735-011@mjcollege.ac.in	*Shaishta Daniya*	*1604-20-735-011*	NO	2	2	2	1	1	1	1
12	1604-20-735-012@mjcollege.ac.in	*Hafsa Jaziba*	*1604-20-735-012*	yes	4	5	5	5	5	5	5
13	1604-20-735-013@mjcollege.ac.in	*Syeda Huzaifah Younus*	*1604-20-735-013*	yes	5	5	4	5	5	3	4
14	1604-20-735-014@mjcollege.ac.in	*Nandyala Kalam Basha*	*1604-20-735-014*	yes	5	3	5	5	5	5	5
15	1604-20-735-015@mjcollege.ac.in	*Mohammed Emad Sultan Siddiqi*	*1604-20-735-015*	yes	5	5	5	4	5	5	5
16	1604-20-735-016@mjcollege.ac.in	*Md Wajahath*	*1604-20-735-016*	yes	4	5	5	5	5	4	5
17	1604-20-735-017@mjcollege.ac.in	*Mahmood Khan*	*1604-20-735-017*	yes	5	5	5	5	5	5	5
18	1604-20-735-018@mjcollege.ac.in	*Mohamed Nawaz Ahmed*	*1604-20-735-018*	yes	3	4	5	5	5	5	5
19	1604-20-735-019@mjcollege.ac.in	*Syed Saffan Ahmed*	*1604-20-735-019*	yes	4	5	4	5	5	5	4
20	1604-20-735-020@mjcollege.ac.in	*Thowheedulla Khan*	*1604-20-735-020*	yes	5	5	5	5	5	5	5
21	1604-20-735-021@mjcollege.ac.in	*Mohammed Mohtasimuddin*	*1604-20-735-021*	yes	5	4	5	5	5	5	5
22	1604-20-735-022@mjcollege.ac.in	*Waheed Khan*	*1604-20-735-022*	yes	5	5	5	5	5	5	5
23	1604-20-735-023@mjcollege.ac.in	*Gore Mohammed Farhan ullah*	*1604-20-735-023*	yes	5	4	5	3	5	5	5
24	1604-20-735-024@mjcollege.ac.in	*Mohammed Amaan Ali*	*1604-20-735-024*	yes	5	5	5	5	5	5	5
25	1604-20-735-025@mjcollege.ac.in	*Mohammad Arbaz*	*1604-20-735-025*	yes	5	5	4	5	5	5	4
26	1604-20-735-029@mjcollege.ac.in	*Mohammed Anas Mahboob Ali*	*1604-20-735-029*	yes	5	5	5	4	5	5	5
27	1604-20-735-030@mjcollege.ac.in	*Syed Khaif Mohiuddin*	*1604-20-735-030*	yes	3	5	5	5	4	4	5
28	1604-20-735-031@mjcollege.ac.in	*Arshad Ahmed Shareef*	*1604-20-735-031*	yes	5	5	4	5	5	5	4
29	1604-20-735-032@mjcollege.ac.in	*Rehan Ahmed*	*1604-20-735-032*	yes	3	5	5	5	5	5	5
30	1604-20-735-033@mjcollege.ac.in	*Mohammed Shahid Ali*	*1604-20-735-033*	yes	4	5	5	4	5	3	5
31	1604-20-735-034@mjcollege.ac.in	*Mohammed Zubair*	*1604-20-735-034*	yes	5	5	5	5	5	5	5
32	1604-20-735-035@mjcollege.ac.in	*Mohammed Mustafa Abrar*	*1604-20-735-035*	yes	5	5	5	5	4	5	5

33	1604-20-735-036@mjcollege.ac.in	Syed Danish Amaan	1604-20-735-036	yes	5	5	5	5	5	5	5
34	1604-20-735-037@mjcollege.ac.in	Mohammed Saif ur Rahman	1604-20-735-037	yes	5	5	5	5	5	5	5
35	1604-20-735-038@mjcollege.ac.in	Md Mahboob Zeeshan	1604-20-735-038	yes	5	5	5	5	5	5	5
36	1604-20-735-039@mjcollege.ac.in	Mohammed Haneef	1604-20-735-039	yes	5	5	5	5	5	4	5
37	1604-20-735-040@mjcollege.ac.in	Mohd Bilal Ahmed	1604-20-735-040	yes	5	5	3	5	3	5	3
38	1604-20-735-041@mjcollege.ac.in	Mohammed Bin Omer	1604-20-735-041	yes	5	5	5	5	4	5	5
39	1604-20-735-042@mjcollege.ac.in	Mohammed Aathif Junaid	1604-20-735-042	yes	5	3	4	4	5	5	4
40	1604-20-735-043@mjcollege.ac.in	Safwan Mohammed	1604-20-735-043	yes	5	5	5	5	5	5	5
41	1604-20-735-046@mjcollege.ac.in	Mohammed Bilal Ahmed	1604-20-735-046	yes	5	5	5	5	5	5	5
42	1604-20-735-047@mjcollege.ac.in	Mir Ahmed Ali	1604-20-735-047	yes	5	5	5	5	5	5	5
43	1604-20-735-048@mjcollege.ac.in	Syed Salluddin	1604-20-735-048	yes	5	3	5	5	5	4	5
44	1604-20-735-049@mjcollege.ac.in	Mohamed Akhtar	1604-20-735-049	yes	5	5	5	5	5	5	5
45	1604-20-735-050@mjcollege.ac.in	Fahat Bar Khan	1604-20-735-050	yes	5	5	5	5	5	5	5
46	1604-20-735-051@mjcollege.ac.in	Mohd Hamza Anwar	1604-20-735-051	yes	4	5	5	4	5	3	5
47	1604-20-735-052@mjcollege.ac.in	Mohammed Maaz Waheed	1604-20-735-052	yes	5	5	5	5	5	5	5
48	1604-20-735-053@mjcollege.ac.in	Syed Anas Mannan Ahmed	1604-20-735-053	yes	5	5	5	5	4	5	5
49	1604-20-735-054@mjcollege.ac.in	Mohammed Farooq	1604-20-735-054	yes	5	5	5	5	5	5	5
50	1604-20-735-056@mjcollege.ac.in	Syed Ibrahim uddin	1604-20-735-056	yes	5	5	5	5	5	5	5
51	1604-20-735-057@mjcollege.ac.in	Syed Yahiya	1604-20-735-057	yes	5	5	5	5	5	4	5
52	1604-20-735-058@mjcollege.ac.in	Mohd Ghouse Tazeem	1604-20-735-058	yes	5	5	3	5	3	5	3
53	1604-20-735-059@mjcollege.ac.in	Syed Rayanuddin	1604-20-735-059	yes	5	5	5	5	4	5	5
54	1604-20-735-060@mjcollege.ac.in	Mir Hasan Ali Abedi	1604-20-735-060	yes	5	3	4	4	5	5	4
55	1604-20-735-061@mjcollege.ac.in	Aiman Jameel	1604-20-735-061	yes	5	5	5	5	5	3	5
56	1604-20-735-062@mjcollege.ac.in	Saniya Khanam	1604-20-735-062	yes	4	3	5	4	5	5	5
57	1604-20-735-063@mjcollege.ac.in	Fouziyah Shirin	1604-20-735-063	yes	5	5	5	5	4	4	5
58	1604-20-735-064@mjcollege.ac.in	Sameeha Hameed	1604-20-735-064	yes	5	5	5	5	5	5	5
59	1604-20-735-065@mjcollege.ac.in	Zeba	1604-20-735-065	NO	1	1	1	1	1	1	1
60	1604-20-735-066@mjcollege.ac.in	Anees unnisa	1604-20-735-066	yes	5	5	5	5	5	5	5
61	1604-20-735-067@mjcollege.ac.in	Maleeha Naba	1604-20-735-067	yes	5	5	5	5	4	5	5
62	1604-20-735-068@mjcollege.ac.in	Hurmath Sara	1604-20-735-068	yes	4	5	5	3	5	4	5
63	1604-20-735-069@mjcollege.ac.in	Zainab Sultana	1604-20-735-069	yes	5	5	4	5	5	5	4
64	1604-20-735-070@mjcollege.ac.in	Zaid Amer Syed	1604-20-735-070	yes	5	5	5	5	4	5	5
65	1604-20-735-071@mjcollege.ac.in	Ayyub Khan	1604-20-735-071	yes	5	5	5	5	5	4	5
66	1604-20-735-072@mjcollege.ac.in	Md Furqan Hasan	1604-20-735-072	yes	4	5	5	5	5	5	5
67	1604-20-735-074@mjcollege.ac.in	Ahsan Baseer	1604-20-735-074	yes	5	3	5	5	5	5	5
68	1604-20-735-075@mjcollege.ac.in	Mohammed Sufyan Saleem	1604-20-735-075	yes	5	5	5	4	5	5	5
69	1604-20-735-076@mjcollege.ac.in	Mohammed Ilyas Ahmed	1604-20-735-076	yes	4	5	5	5	5	4	5

70	1604-20-735-077@mjcollege.ac.in	Syed Rehan Malik	1604-20-735-077	yes	5	5	5	5	5	5	5
71	1604-20-735-078@mjcollege.ac.in	Hasan Ali Al Qattan	1604-20-735-078	yes	3	4	5	5	5	5	5
72	1604-20-735-079@mjcollege.ac.in	Mohammed Nabeel	1604-20-735-079	yes	4	5	4	5	5	5	4
73	1604-20-735-081@mjcollege.ac.in	Quazi Zainuddin Ahmed Siddiqui	1604-20-735-081	yes	5	4	5	5	5	5	5
74	1604-20-735-082@mjcollege.ac.in	Faraaz Siddiqui	1604-20-735-082	yes	5	5	5	5	5	5	5
75	1604-20-735-083@mjcollege.ac.in	Shaik Fayaz Ahmed	1604-20-735-083	yes	5	4	5	3	5	5	5
76	1604-20-735-084@mjcollege.ac.in	Mohammed Irfan Khan	1604-20-735-084	yes	5	5	5	5	5	5	5
77	1604-20-735-085@mjcollege.ac.in	Syed Khaja Fakhruddin	1604-20-735-085	yes	5	5	4	5	5	5	4
78	1604-20-735-086@mjcollege.ac.in	Mohammed Faizan Ahmed	1604-20-735-086	yes	5	4	2	5	4	5	2
79	1604-20-735-087@mjcollege.ac.in	Omer Farooq	1604-20-735-087	yes	4	5	5	5	5	5	5
80	1604-20-735-088@mjcollege.ac.in	Ghulam Ahmed Ibraaz Mohiuddin	1604-20-735-088	yes	5	4	4	5	5	5	4
81	1604-20-735-090@mjcollege.ac.in	Mohammed Faizan Shah	1604-20-735-090	yes	3	5	5	5	4	4	5
82	1604-20-735-091@mjcollege.ac.in	Mohammed Hassan Ahmed	1604-20-735-091	yes	5	5	4	5	5	5	4
83	1604-20-735-092@mjcollege.ac.in	Mohammed Salahuddin	1604-20-735-092	yes	3	5	5	5	5	5	5
84	1604-20-735-093@mjcollege.ac.in	Mohd Gufran Khursheed	1604-20-735-093	yes	4	5	5	4	5	3	5
85	1604-20-735-094@mjcollege.ac.in	Mohd Mehraj Ahmed	1604-20-735-094	yes	5	5	5	5	5	5	5
86	1604-20-735-095@mjcollege.ac.in	Mohammed Sami uddin	1604-20-735-095	yes	5	5	5	5	4	5	5
87	1604-20-735-096@mjcollege.ac.in	Syed Imtiyaz Ali	1604-20-735-096	yes	5	5	5	5	5	5	5
88	1604-20-735-097@mjcollege.ac.in	Anzar Irfan Khan	1604-20-735-097	yes	5	5	5	5	5	5	5
89	1604-20-735-098@mjcollege.ac.in	Sk Khadir Pasha	1604-20-735-098	yes	5	5	5	5	5	5	5
90	1604-20-735-099@mjcollege.ac.in	Mohd Zahed Khan	1604-20-735-099	yes	5	5	5	5	5	4	5
91	1604-20-735-100@mjcollege.ac.in	Hamzah Habeeb Iqbal	1604-20-735-100	yes	5	5	3	5	3	5	3
92	1604-20-735-101@mjcollege.ac.in	Mirza Sameeullah Baig	1604-20-735-101	yes	5	5	5	5	4	5	5
93	1604-20-735-102@mjcollege.ac.in	Huzaifa Abdul Wadood Siddiqui	1604-20-735-102	yes	5	3	4	4	5	5	4
94	1604-20-735-103@mjcollege.ac.in	Farhan Ahmed	1604-20-735-103	yes	5	5	5	5	5	5	5
95	1604-20-735-104@mjcollege.ac.in	Syed Arhhann Ahmad	1604-20-735-104	yes	5	5	5	5	5	5	5
96	1604-20-735-105@mjcollege.ac.in	Mohammed Amaan Ali	1604-20-735-105	NO	2	2	2	1	1	1	2
97	1604-20-735-106@mjcollege.ac.in	Syed Haseeb uddin	1604-20-735-106	yes	5	5	5	5	5	5	5
98	1604-20-735-110@mjcollege.ac.in	Shaik Irshad Ahmed	1604-20-735-110	yes	5	5	5	5	5	5	5
99	1604-20-735-111@mjcollege.ac.in	Mohammad Abdul Arshad	1604-20-735-111	yes	4	5	5	4	5	3	5
100	1604-20-735-112@mjcollege.ac.in	Abdul Quadir Omer	1604-20-735-112	yes	5	5	5	5	5	5	5
101	1604-20-735-113@mjcollege.ac.in	Mohd Abdullah Sobaan	1604-20-735-113	yes	5	5	5	5	4	5	5
102	1604-20-735-114@mjcollege.ac.in	Abdullah Khan	1604-20-735-114	yes	5	5	5	5	5	5	5
103	1604-20-735-115@mjcollege.ac.in	Mohd Mirza Asgar Hadi	1604-20-735-115	yes	5	5	5	5	5	5	5
104	1604-20-735-116@mjcollege.ac.in	Mohammed Adnan	1604-20-735-116	yes	5	5	5	5	5	3	5

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105	1604-20-735-117@mjcollege.ac.in	***Mohd Adnan Pasha***	***1604-20-735-117***	yes	4	3	5	4	5	5	5
106	1604-20-735-118@mjcollege.ac.in	***Syed Ahmed Khasim Ghouri***	***1604-20-735-118***	yes	5	5	5	5	4	4	5
107	1604-20-735-119@mjcollege.ac.in	***Makhan Vishal Singh***	***1604-20-735-119***	yes	5	5	5	5	5	5	5
108	1604-20-735-120@mjcollege.ac.in	***Syed Nawaz***	***1604-20-735-120***	NO	3	3	3	2	2	2	1

Feebback Questions
It was excellent
The workshop met your Expectations
Your level of knowledge at the start of the workshop
How satisfied were you with the session content?
The tutor was open to new ideas and view points
The tutor took account of students existing knowledge and level of understanding
Adequacy of slides in terms of coverage of workshop
Precision and answering the questions by the tutor

30/03/22

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Outcome of Workshop.

Many students have done mini project based on the knowledge what gained from 2 week workshop : Internet of things.

1. Introduction to Node MCU
2. Installation of arduino IDE
3. Programming the microcontroller for IOT platform
4. Perform the Led blink and Atmospheric temperature monitoring using the microcontroller
5. Designing of Smart dust bin using Microcontroller
6. Familiarity with the Raspberry pi
7. Installation of OS on Raspberry pi
8. Programming R pi for LED blink and Temperature Monitoring
9. Programming R PI for UV sensor
10. Familiarity with the Thing speak

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Department Of Electronics and Communication Engineering

In Collaboration with

IEEE Student Branch MJCET and MJCET Institute Innovation Council

Report

Date: 21/12/2020

One Week Skill Development Program (SDP) on Digital System Design

A one Week Skill Development Program (SDP) on Digital System Design organized Workshop on a **"One Week Lab Intensive Training Programme"** in **"Digital System Design using Verilog HDL"** from 30th December 2020 to 4th January 2021" was conducted by MJCET in the Department Of Electronics and Communication Engineering.

As part of this Programme two workshops are organized. Registration fees is 100/- Total 14 MJCET BE ¾ ECE students registered to this workshop

Workshop Coordinator: Dr Mohammed Sabir Hussain, Asst Professor ECED

Teaching Assistant: Mr. Moiz, Mr. Mohd Sohel and Mr. Fasiullah.

No of Participants Registered are : 14

Number of participants attended: 14

Group photo of the workshop, detail timetable schedule of Workshop and attendance sheet have been enclosed.

30/05/2021

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Date: 21/12/2020

To
Head of the Department,
Electronics & Communication Engineering Dept,
Muffakham Jah College of Engineering & Technology,
Hyderabad.

Sub: Permission to organize Seminar on **"One Week Lab Intensive Training Programme"** in **"Digital System Design using Verilog HDL"** -Reg

Sir,

I am pleased to inform you that Seminar on **"One Week Lab Intensive Training Programme"** in **"Digital System Design using Verilog HDL"** for the Students of E.C.E is scheduled.

Schedule as follows.

Date	30/12/2020
Title of Seminar	**"One Week Lab Intensive Training Programme"** in **"Digital System Design using Verilog HDL"**
Resource Person	Dr.Arifuddin Sohel, Prof & Head, ECED Dr. Sabir Hussain , Associate Professor. ECED
Participants	B.E II,III Year Students

So, I request you to grant the permission to conduct the SDP in the DSP Lab

Faculty Incharge

Dr. Sabir Hussain,

Associate Professor

30/03/2021

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One Week Lab Intensive Training Programme on Digital System Design Using Verilog HDL Workshop Schedule

Date	Contents
30-12-20 (Monday)	Introduction to verilog HDL, EDA Tool Demonstration (ModelSim)
	.Introduction to Combinational and Sequential Circuits
	HDL Design using Gate level modeling
31-12-20 Tuesday	HDL Design using Dataflow level modeling
	HDL Design using Behavioral modeling – Flip flops , Counters FSM Charts-Mealy and Moore
02-01-21 Thursday	Advanced Verilog HDL Concepts
03-01-21 Friday	Advanced Verilog HDL Concepts
04-01-21 Saturday	System Verilog Concepts Quiz

30/03/2021
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Meeting Minutes:

One Week Lab Intensive Training Programme on
Digital System Design Using Verilog HDL
Workshop Schedule

Meeting Minutes of committee members – 22/12/2020 – HOD Room

Attended by

1. Dr. Arifuddin Sohel, Prof & Head ,ECED
2. Dr. Kaleem Fatima
3. Dr. Ayesha Naaz
4. Dr. Sabir Hussain , Workshop Coordinator
5. Dr. MA Raheem , Workshop Co- Coordinator

Minutes

The Committee discussed topics to cover in this workshop as per industry requirements and resource persons to cover the technical topics.

Speakers:

Dr. Arifuddin Sohel, Prof & Head ,ECED,MJCET

Dr. Sabir Hussain, Associate Professor , ECED,MJCET

20/03/2022
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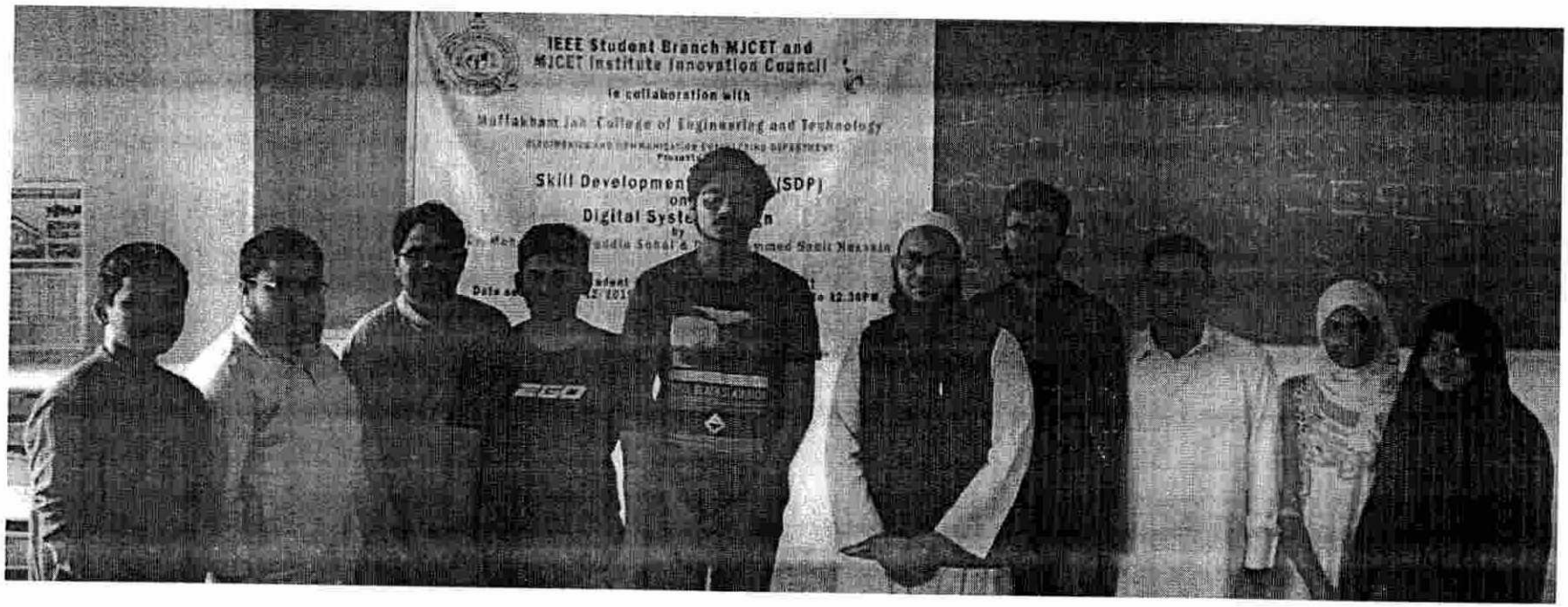

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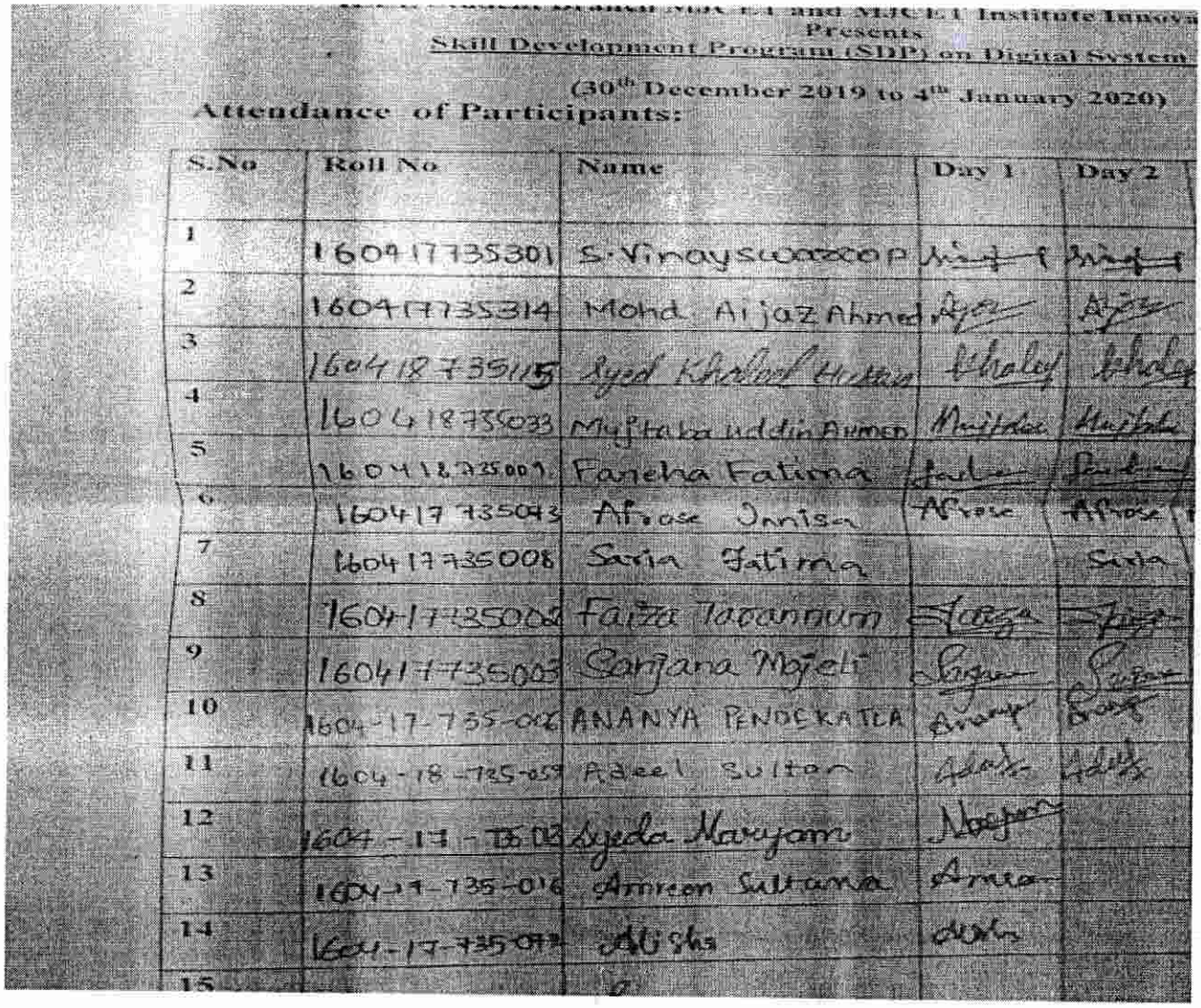
Attendance:



Presents

Skill Development Program (SDP) on Digital System

(30th December 2019 to 4th January 2020)

Attendance of Participants:

S.No	Roll No	Name	Day 1	Day 2
1	160917735301	S. Vinay Swaroop		
2	160917735314	Mohd. Aijaz Ahmed		
3	160918735115	Syed Khaleel Hussain		
4	160918735033	Mujtaba uddin Ahmed		
5	160918735009	Fareha Fatima		
6	160917735043	Afroze Jnnisa		
7	160917735008	Saria Fatima		
8	160917735002	Faiza Tabassum		
9	160917735003	Sanjana Majeti		
10	160917735042	ANANYA PENDEKATLA		
11	160918735059	Abdul Sultan		
12	160917735023	Sajeda Maryam		
13	160917735016	Ameen Sultana		
14	160917735044	Alisha		
15				

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Certificates:

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Electronics and Communication Engineering Department
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Skill Development Program on Digital System Design
30th December 2019 to 4th January 2020

Certificate of Participation

This is to certify that

has participated in the Skill Development Program (SDP) on Digital System Design held from 30th December 2019 to 4th January 2020, Organized by ECE Department, MJCET in association with IEEE Student Branch MJCET and MJCET Institute Innovation Council.

Dr.Mohammed Sabir Hussain
SDP Coordinator

Dr. Mohammed Arifuddin Sohel
Professor and Head, ECED
Branch Counselor, IEEE MJCET SB

Dr. Basheer Ahmed
Advisor cum Director, MJCET

CAS

Outcome of SDP:

The outcomes of skill development program on "Digital System Design Using Verilog HDL" are the participants able to develop Verilog HDL code for digital circuits using data flow, structural modelling and develop test-benches. Participants are able to simulate and verify the functionality of the module using ModelSim.

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